Name of Paper	**:**	**Digital Systems and Applications**
Name of the Course	**:**	**B.Sc. (Hons.) Physics**
Semester	**:**	**III**
Duration	**:**	**3 Hours**
Maximum Marks	**:**	**75**

Dec. 2019

Question No. 1 is compulsory.

Answer any four of the remaining six,
attempting any two parts from each questions.

Q. 1. Attempt all parts of this questions :

(*i*) Why two state operations is preferred for designing digital circuits? Name two devices that you see around which exhibit two states. (3)

Ans. Digital circuit is based on the design that every signal in a circuit is either in the state of 'on' or 'off'. The two states literally means 'binary'. The reason for chosing this design is that it greatly simplifies engineering of electronic circuits. In reality, electrical signals can not change state from 0V to 5V in an instant. It takes some time wires are not perfectly conductors. Every wire acts as a small antenna and emit radio waves and that radio waves are picked by other wires which also acts of a antenna within a wire current bounos whenever its reaches a spot which is different from the rest of the wire. From electrical point of views, this gets extremelly complicated to manage and it becomes almost impossible to design a circuit that would operate at high speeds and law power.

Two devices : Switches and capacitor.

(*ii*) Draw the circuit of a NOT gate using transistor and explain its working. (2)

Ans. The solution to this questions is in your textbook.

(*iii*) What do you understand by an instruction cycle and a machine cycle in 8085 microprocessor ? (3)

Ans. The time required to execute and fetch and entire instruction is called instruction cycle. It consists of :

(*a*) Fetch Cycle : The next instruction is fetched by the address stored in Program Counter (PC) and then stored in the instruction register.

(*b*) Decode Instruction : Decoder interprets the incoded instruction from instruction register.

(*c*) Reading Effective Address : The address given in instruction is read from main memory and required data is betched. The effective address depends on direct addressing mode or indirect addressing mode.

(*d*) Execution Cycle : Consists Memory Read (MR), Memory Write (MW), input output read (IOR) and input output write (IOW).

The time required by the microprocess or to complete an operation of accessing memory or input/output device is called machine cycle.

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(*iv*) Apply the duality theorem to the following expression : **(2)**

(*a*) A(B + C) = AB + AC **(*b*) $A + \overline{A}B = A + B$**

Ans. (*a*) A (B + C) = AB + AC

The duality theorem states.

(*i*) changing each OR sign to an AND sign.

(*ii*) Changing each AND sign to OR sign.

(*iii*) Complementing any 0 or 1 appearing in expression.

So, above expression now

$$A + BC = (A + B)(A + C)$$

(*b*) $$A + \overline{A}B = A + B$$

After duality theorem it becomes

$$A + (\overline{A} + B) = A . B$$

(*v*) Subtract 11001101 from 10110101 using 2's complement method. **(3)**

Ans. The solution to this questions is in your textbook.

(*vi*) What is the role of control voltage pin in IC 555 timer ? **(2)**

Ans. The solution to this questions is in your textbook.

(*vii*) Draw block diagram of a RAM chip and explain the role of each pin. **(3)**

Ans. The solution to this questions is in your textbook.

Q. 2. (*i*) (*a*) What do you understand by Digital and Linear ICs? Give two examples of each. **(4)**

(*b*) In an oscilloscope, a 100 V signal produces a deflection of 2 cm corresponding to a certain setting of vertical gain control. If another voltage produces 7.3 cm deflection for the same setting of the vertical gain control, what is the value of the voltage ? **(3)**

Ans. (*a*) The solution to this questions is in your textbook.

(*b*) $V_1 = 100V$, deflection $= d_1 = 2$ cm

$\lambda_2 = 7.3$ cm, $V_2 = ?$

Voltage per deflection should be same.

$$\frac{V_1}{d_1} = \frac{V_2}{d_2}$$

$$\frac{100}{2} = \frac{V_2}{7.3} \Rightarrow V_2 = \frac{7.3 \times 100}{2}$$

$$V_2 = 365 \text{ V}$$

(*ii*) Perform the following conversion :

(*a*) $(198.25)_{10}$ into Binary number and Hexadecimal number. **(4)**

(*b*) $(324.24)_{10}$ into Octal number. **(3)**

Ans. (*a*) The solution to this questions is in your textbook.

(*b*) The solution to this questions is in your textbook.

(*iii*) An three variable truth table produce logic 1 output when the number of Truth Table for the problem considering the output as don't care for the terms for

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which the decimal equivalent of the input variables is 0, 1 and 2. Determine the simplest SOP equation for this truth table using K-Map method and design the logic circuit for the function using NAND gates and XOR gates only. **(7)**

Ans.

A	B	C	Y
0	0	0	X
0	0	1	X
0	1	0	X
1	0	0	0
0	1	1	1
1	0	1	1
1	1	0	1
1	1	1	0

where, X is don't care condition.

K–Map

	$\overline{C}$	C
$\overline{A}\,\overline{B}$	X	X
$\overline{A}\,B$	X	0
$A\,B$	1	0
$A\,\overline{B}$	0	1

X is don't care → which means we can table it as 0 or 1, whichever gives simpler circuit.

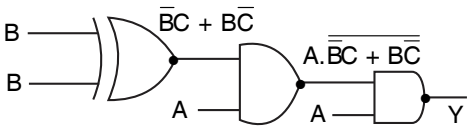
We will take it as 1.

$$Y = \overline{A} + A\overline{B}\,\overline{C} + A\overline{B}C$$

$$Y = \overline{A \,.\, A.\,(\overline{B}C + B\overline{C})}$$

Using $\overline{A \,.\, B} = \overline{A} + \overline{B}$

$$Y = \overline{A}\;\overline{A \,.\, (\overline{B}C + B\overline{C})}$$



So, $Y = \overline{A} + A.\,(\overline{B}\,C + B\overline{C})$

Q. 3. (*i*) (*a*) Draw truth table and block diagram of a full subtractor circuit using half subtractors. **(4)**

(*b*) The SUB input control signal of a full adder/subtractor circuit is connected to the output of a 4-input XOR gate. Tabulate the combinations of XOR gate input variable for which the adder/subtractor circuit perform the task of (*i*) Addition and (*ii*) Subtraction. **(3)**

Ans. (*a*) The solution to this questions is in your textbook.

(*b*) The solution to this questions is in your textbook.

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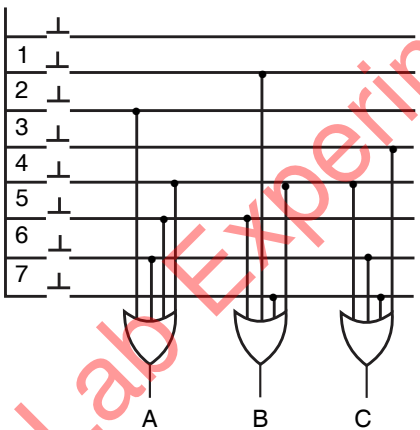
(*ii*) Design an encode which generates the following truth table : **(7)**

Input	Output
Y_1	A B C
0	0 0 0
3	0 0 1
1	0 1 0
7	0 1 1
2	1 0 0
6	1 0 1
5	1 1 0
4	1 1 1

Ans. (*ii*) En codes

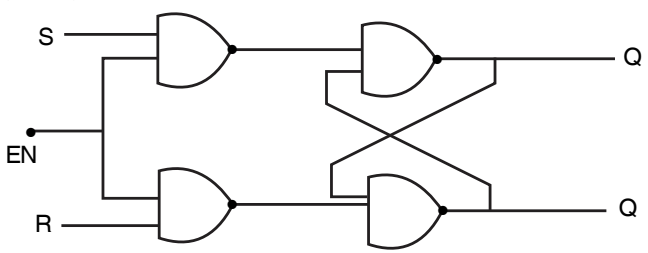


(*iii*) Design a 4-bit serial-in-parallel-out shift right register using negative edge triggered D flip-flops. Display the timing diagram to store 4-bit binary number $(1101)_2$ assuming the register is initially all clear. How many number of clock pulses are required to store the number ? **(7)**

Ans. The solution to this questions is in this textbook.

Q. 4. (*i*) Draw the circuit of a clocked SR latch using NAND gates and explain its working. Why the S = 1 and R = 1 is called the forbidden condition ? **(7)**

Ans.



Clocked RS latch using NAND Gate

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Truth table :

EN	S	R	Q_{n+1}	
1	0	0	Q_n	(no change)
1	0	1	0	
1	1	0	1	
1	1	1	?	(illegal)
0	X	X	Q_n	(no change)

Working : When the enable input is high, information at the R and S inputs will be transmitted directly to the outputs. The latch is said to be inafled. The output changes in response to input changes as long as the ENABLE is high. When the ENABLE input goes law, the output will ration the information that was present on the input when the high to low transition took place. In this way it is possible to strobe or cook the flip-flop in order to store in formation (set it or reset it) at any time and then hold the stored information for any desired period of time. This flip-flop is called *w* gated or clock RS flip-flop or latch. Now, there are three input R, S and ENABLE or clock input, EN. Notice that the truth table output is Q_{n+1} not Q_n. The is because we must considertwo different instants in to,e, the time before the ENABLE goes low Q_n and the time just after ENABLE goes low Q_{n+1}.

When EN = 0, the Flip-flop is disabled and R and S have no effect thus the truth table entry for R and S is X (don't (ore).

The case R = 1 and S = 1 is called forbidden because it forces the both output Q and $\overline{Q}$ equal to 1; which is not possible.

(*ii*) (*a*) Draw circuit diagram of a JK latch (using NAND gates) and discuss its truth table. (4)

(*b*) Mention the methods by which the race around conditions is avoided in latch. (3)

Ans. (*a*) The solution to this questions is in your textbook.

(*b*) The solution to this questions is in your textbook.

(*iii*) Design a MOD-8 asynchronous down counter using negative edge triggered JK flip-flops. Draw the timing diagram of the counter assuming the initial state as 0000 and that the propagation delay of each flip-flop is 10 ns. The time period of the input clock pulse is 100 ns. (7)

Ans. The solution to this questions is in your textbook.

Q. 5. (*i*) An instruction (MOV C, A) with the hex code 4F H is stored in the memory location 2006 H. Discuss the steps taken by the microprocessor in order to execute this instruction. What would be the content of the program counter (PC) register after the execution of this instruction ? (7)

Ans. The solution to this questions is in your textbook.

(*ii*) Explain with a timing diagram the following operation : (7)

Memory Location	M/Code	Mnemonic
2000	06	MVI B, 52H
2001	52	

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Ans. The solution to this questions is in your textbook.

(*iii*) A memory bank uses a 16-line address bus and 8-line data bus. The first 32 KB of the memory is allocated to two ROM's of 16 KB each, and the remaining space to the RAM's of 8KB each. Write down the initial and final addresses of each chip in the entire memory map.

Ans. 16 – address line can identify :

$$2^{16} = 64\ kB \text{ locations}$$

The space allocated to different memory locations

$$16\ kB + 16\ k\,B + 8k\,B + 8k\,B + 8\ kB + 8kB$$

Initial and final address for first ROM

$$\left.\begin{array}{l} 2^{\circ} \rightarrow \text{For initial address} \\ 2^{4} \rightarrow \text{For final address} \end{array}\right] \rightarrow \text{First } 16\ k\,B \text{ ROM}$$

In second 16 k B ROM

$$\left.\begin{array}{l} 16\ k\ B + 1 \rightarrow \text{For initial address} \\ 2^{5} = 32\ k\,B \rightarrow \text{For Final address} \end{array}\right] \rightarrow \text{Next } 16\ k\,B \text{ ROM}$$

For first 8 k B RAM :

$$\left.\begin{array}{l} (32\ k\ B + 1) \rightarrow \text{For initial address} \\ 40\ k\ B \rightarrow \text{For final address} \end{array}\right] \rightarrow \text{First } 8\ k\,B \text{ RAM}$$

For third 8 k B RAM

$$\left.\begin{array}{l} (48\ k\ B + 1) \rightarrow \text{For initial address} \\ 56\ k\ B \rightarrow \text{For final address} \end{array}\right] \rightarrow \text{Third RAM}$$

For fourth 8 k B RAM

$$\left.\begin{array}{l} (56\ k\ B + 1) \rightarrow \text{Initial address} \\ 64\ k\ B \rightarrow \text{Find address} \end{array}\right] \rightarrow \text{Fourth RAM}$$

Q. 6. (*i*) (*a*) What are flags ? If the accumulator contains 0BH and register C contain 05H, which flags are affected when CMP C is executed. (3)

(*b*) If the clock frquency of a microprocessor is 5MHz, how much time is required to execute an instruction of 7 T states ? (4)

Ans. (*a*) The flag register is a sprcial purpose register. Depending on the value of refult after any arithmetic and logical operation the flag bits become set (*i*) or (0). In 8085 microprocess or flag register consists of 8 bits and only 5 of them are useful. The five flags are

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z		AC		P		CY

1. Sign flag (S)
2. Zero flag (Z)
3. Awallary carry flag (AC)
4. Parity flag (P)

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5. Carry flag (CY)

Accumulator = A = OBH

Register C = 05 H

C M P C = Compare C

Before execution, A = OBH C = 05H

After execution, A = OBH C = 05H

Since, A is greater than C.

So Both CY and zero flag are reset.

So, CY = 0, Z = 0

(*b*) Clock frequency = $f = 5$ MHz

$= 5 \times 10^6$ HZ

time required for 1 state = $t = \frac{1}{f} = \frac{1}{5 \times 10^6}$

$= \frac{10}{5 \times 10^7} = 2 \times 10^{-7}$ sec

time required for 7T states = $7 \times 2 \times 10^{-7}$ sec.

time = 1.4×10^{-6} sec.

(*ii*) What are the various general purpose registers present in microprocessor 8085 and explain their function? What is the role of program counter (PC) and stack pointer (SP) registers ? **(7)**

Ans. The solution to this questions is in this textbook.

(*iii*) Write an assembly language program to subtract 5DH from FCH stored in memory locations 2006H, respectively using indirect addressing mode. The difference is to be stored in the memory location 2008H and borrow in 2009H. **(7)**

Ans. The solution to this questions is in this textbook.

Q. 7. (*i*) Design an astable multivibrator circuit using IC 555 timer with the following specifications. The time period of the output waveform is 100 ms duty cycle is 80%. Draw the output waveform and the voltage across the capacitor. **(7)**

Ans. The solution to this questions is in this textbook.

(*ii*) (*a*) Give the truth table of XOR and XNOR gates and explain their working as odd even parity detectors. **(4)**

(*b*) Discuss and explain the principle of error detection using parity method. What is the limitation of this method ? **(3)**

Ans. (*a*) The solution to this questions is in this textbook.

(*b*) The solution to this questions is in this textbook.

(*iii*) A 5 MHz and 10 MHz square wave signal is fed to the J and K inputs of a JK flip-flop. Draw the timing diagram for the output Q assuming that the flip-flop is active all the time and initially clear. **(7)**

Ans. The solution to this questions is in this textbook.

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