Free Study Material from All Lab Experiments

Electronics for NET/Gate Physical Sciences # Sequential Circuit

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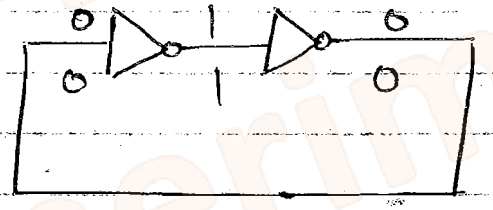
Sequential Circuit

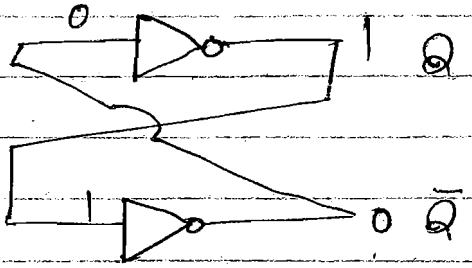
Flip-Flop :-

This is the basic memory element in the digital system. The basic flip-flop is also called Bistable multivibrator It is a single bit storage device. i.e it can store either 1 or 0.

A Flip-Flop can store indefinitely unless and untill the input conditions are changed.



Every Flip-Flop will have two output both will be compliment of each other.



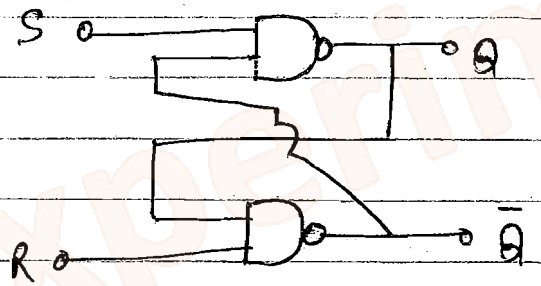
Every Flip-Flop will have cross-coupling in between input and output.

Types of Flip-Flop

1. Latch
2. S.R Flip-Flop
3. JK Flip-Flop
4. D-Flip-Flop
5. T-Flip-Flop

* Difference between Latch and Flip-Flop :-

* Replace every not gat by using NAND gate.



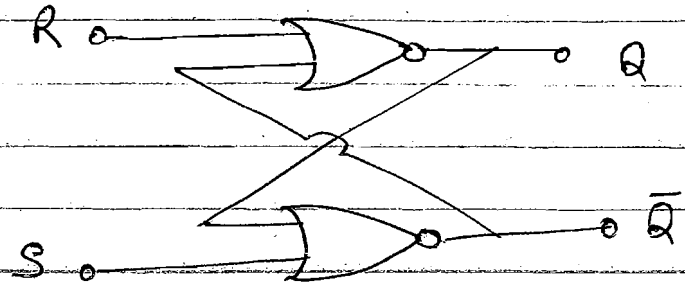
S-R Latch

Truth Table:-

S	R	Q
0	0	Invalid o/p
0	1	1
1	0	0
1	1	previous o/p.

Complementary S-R Latch :-

Replace every NAND gate by NOR gate and interchange either the position of S-R or Q & $\bar{Q}$

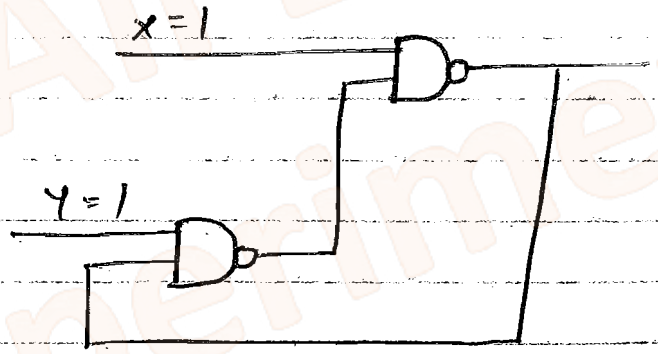


Truth Table :-

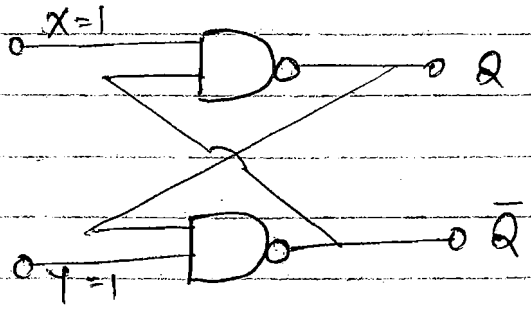
S	R	Q
0	0	Previous Output
0	1	0
1	0	1
1	1	invalid

S-R Flip-Flop :-

Ques Find the output Q for the given circuit.

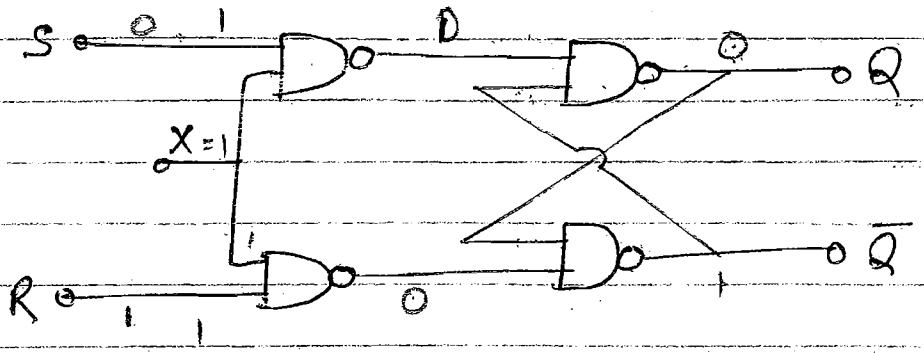


Soln :-



Previous o/p.

* S-R Flip-Flop :-



Truth Table :-

X	S	R	Q
0	X	X	Previous state
1	0	0	Previous State
1	0	1	0
1	1	0	1
1	1	1	Invalid

The disadvantage of SR-Flip Flop is when S=R=1 produces invalid output can't be use for practical applications.

Flip - Flop

- Characteristic Table (o/p Table)
- Charateristic Equation (o/p eqn)
- Exitation Table (i/p Table)

Characteristic Table :-

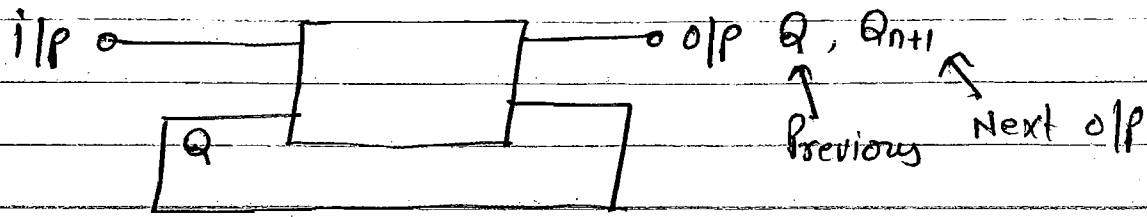
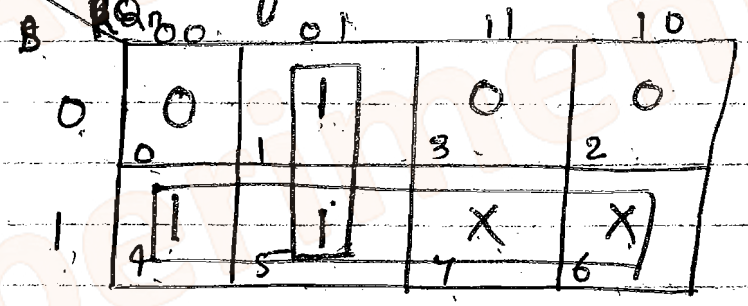


Table { Truth Table } :-

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	X	0
0	1	X	0
1	0	X	1
1	0	X	1
1	1	0	X
1	1	1	X

* Characteristic Equation :-

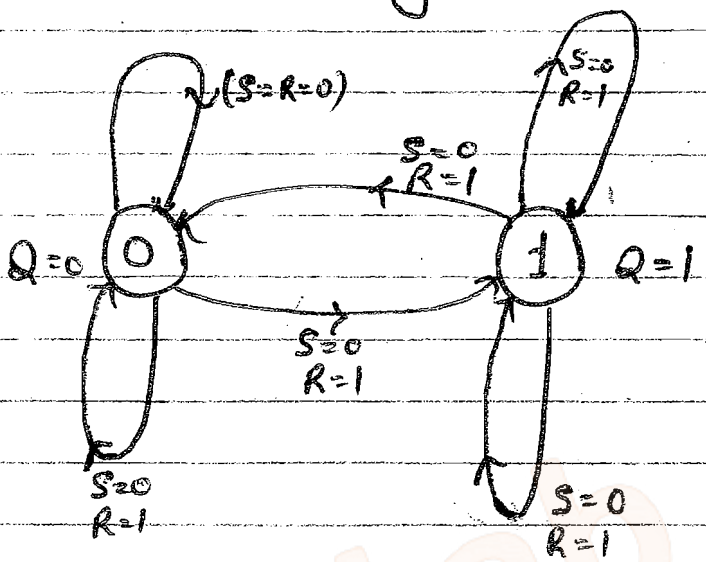


$$Q_{n+1} = S + \bar{R} Q_n \quad \text{---} \circledast \quad \{\text{remember}\}$$

* Exitation Table :-

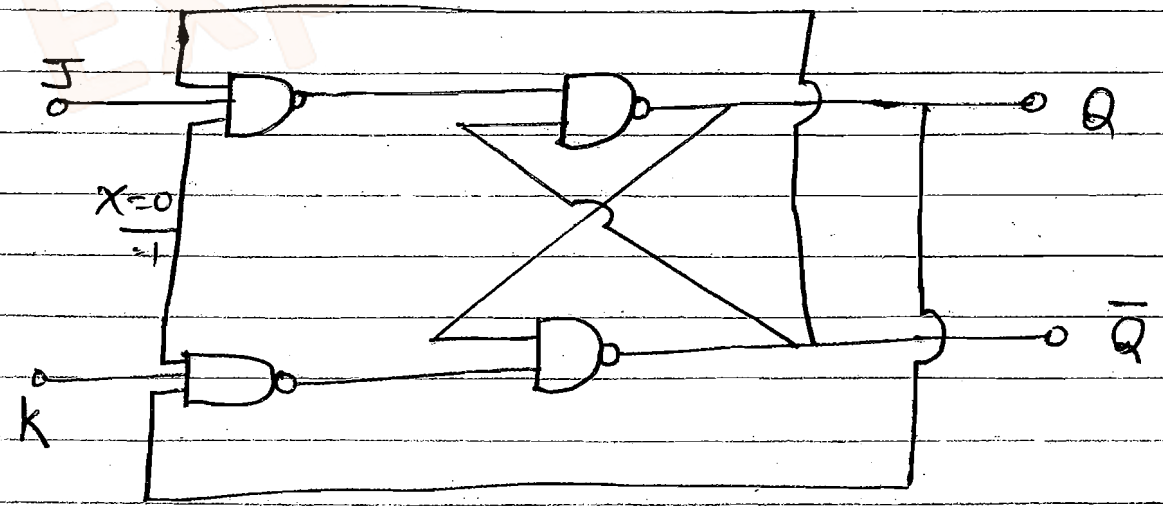
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

* State Transition Diagrams :-



* The Disadvantage of S-R flip-flop is when S=R=1 produces invalid o/p hence replaced by J-K Flip-Flop.

JK-Flip Flop :-



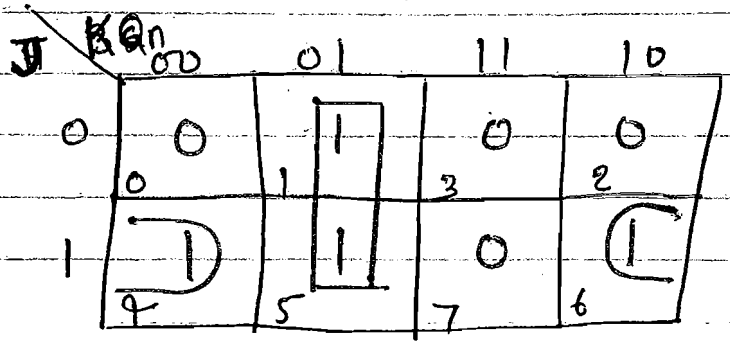
* Truth Table :-

X	J	K	Q
0	X	X	Prev.
1	0	0	Prev.
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}$

* Characteristic Table :-

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

* Characteristic Equation :-



$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

{Remember this}

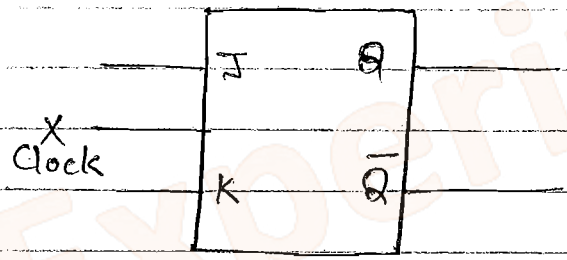
Ques | Draw the exitation table of Jk-Flip-Flop.

Soln

Q_n	Q_{n+1}	J	k
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

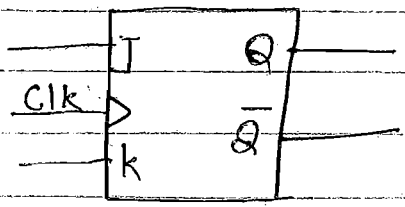
Note :- Jk-Flip-Flop is also called as universal Flip-Flop.

Rectangular box of J-K flip-Flop :-

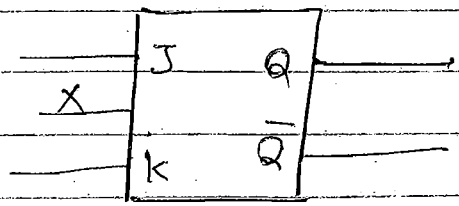


X → Clk works when X = 1
→ does not work X = 0

Meaning of X :- Clock which carry on the J.K Flip-Flop.



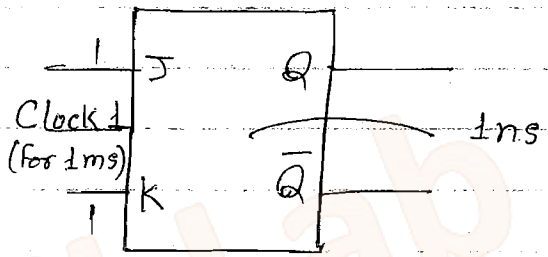
edge triggered Clock pulse

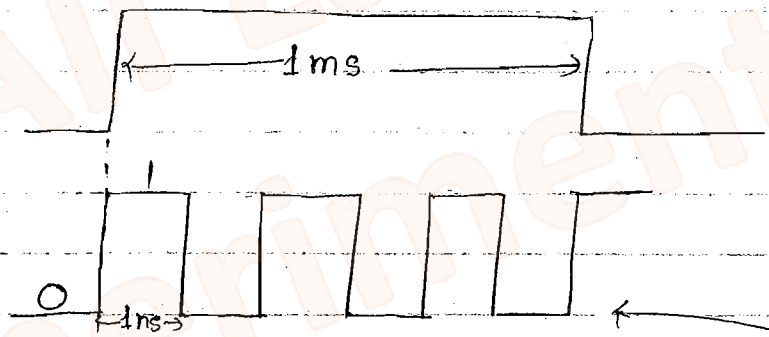


level triggered Clock pulse.

Output changes continuously under the clock pulse as input changes.

In the edge trigger clock pulse output will change either raising edge or falling edge. not both.



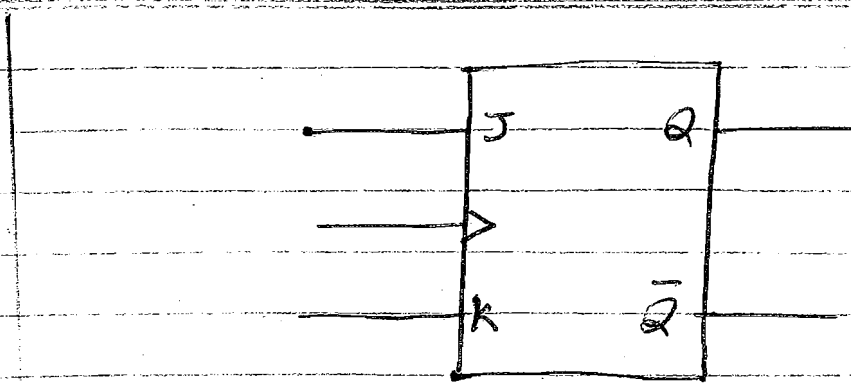


Race Arround Condition.

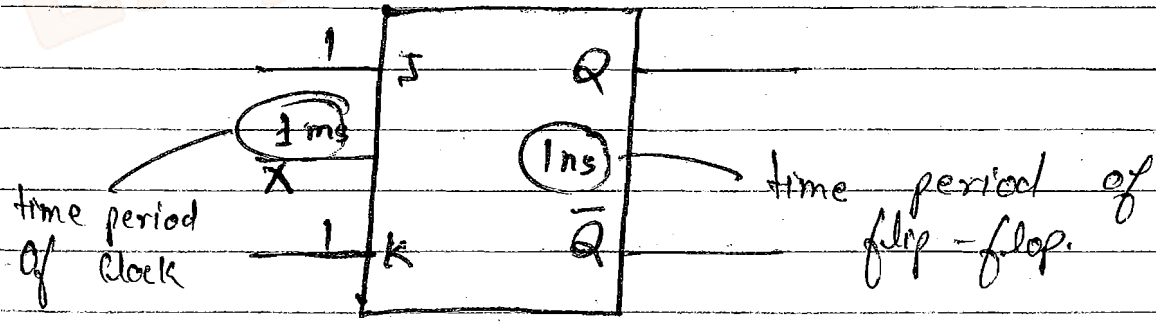
In the level triggered JK-flip-flop output changes many times under a single clock pulse for JK = 1 is called as **Race Arround Condition.**

Race arround condition is the disadvantage of JK-flip flop.

* **Removal of Race Arround Condition:-**



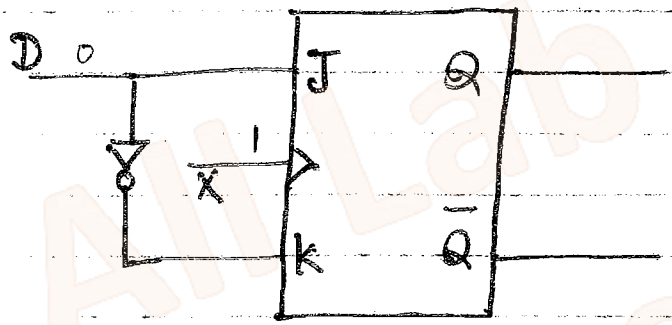
Race arround condition can be removed by using edge triggered clock pulse in place of level triggered clock pulse.



Race arround condition can be removed by reversing the condition $t_{pd\ clk} > t_{pd\ ff}$ to $t_{pd\ clk} < t_{pd\ ff}$.

To increase the time period of flip-flop cascading of flip-flop is performed for example master slave flip flop is also useful for Race arround condition.

* D - Flip Flop :-



Truth table :-

X	D	Q
0	X	Previous
1	0	0
1	1	1

Characteristic Table :-

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Characteristic Equation :-

$$Q_{n+1} = D$$

D - flip-flop acts as a buffer.

⇒ D - flip-flop is useful for implimentation of registers.

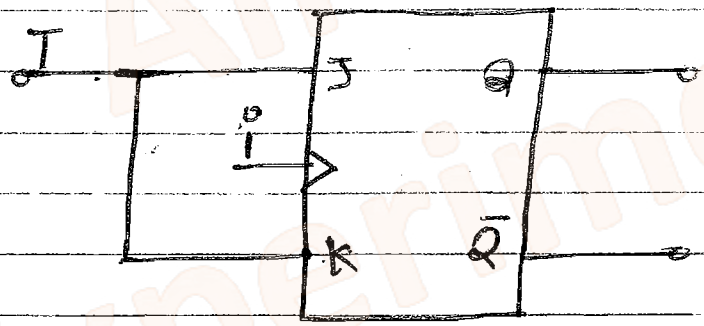
$= J\bar{Q}_n + \bar{K}Q_n$

$= D$

Excitation Table :-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

* T - Flip - Flop



Truth Table :-

X	T	Q
0	X	Previous State
1	0	Previous State
1	1	$\bar{Q}$

Characteristic Table :-

T	Q_n	Q_{n+1}
0	0	Previous (0)
0	1	1
1	0	1
1	1	0

Characteristic Equation :-

$$Q_{n+1} = T \oplus Q_n$$

Exitation Table :-

Q	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

T-Flip Flop perform ex-OR operation :-

* Point To be Remember :-

Characteristic Eqn :-

① SR $Q_{n+1} = S + \bar{R} Q_n$

② JK $Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$

③ D $Q_{n+1} = D$

④ T $Q_{n+1} = T \oplus Q_n$

* Exitation Table :-

Q_n	Q_{n+1}	S	R	J	K	D	T
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	0	1
1	1	X	0	X	0	1	0

For X = 1

J	K	Q
0	0	Previous
0	1	0
1	0	1
1	1	$\bar{Q}$

For X = 1

S	R	Q
0	0	Previous
0	1	0
1	0	1
1	1	X

* Registors :-

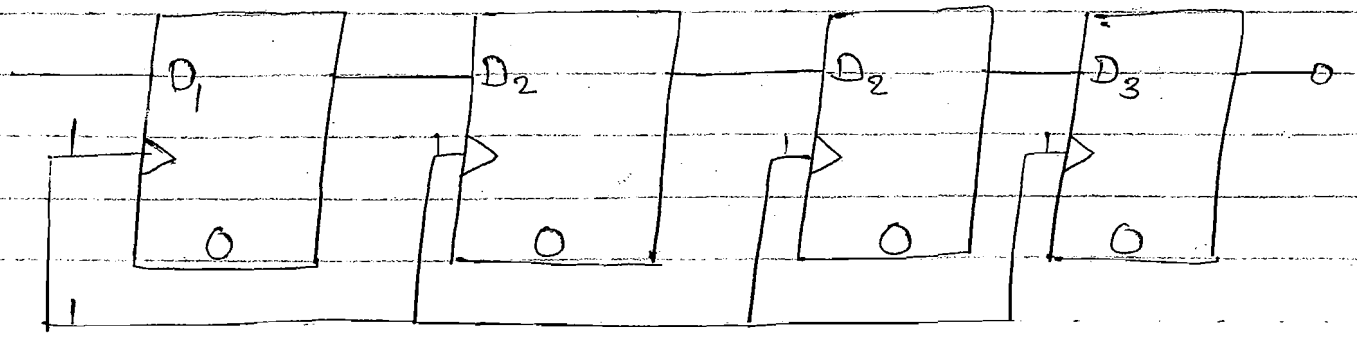
Mainly implimented by D flip-flop.

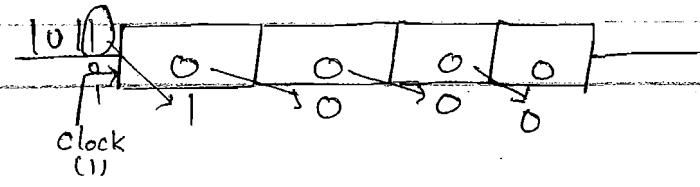
To store n number of bit, n flip-flops are require {because one flip-flop stores only 1 bit either 0 or 1}.

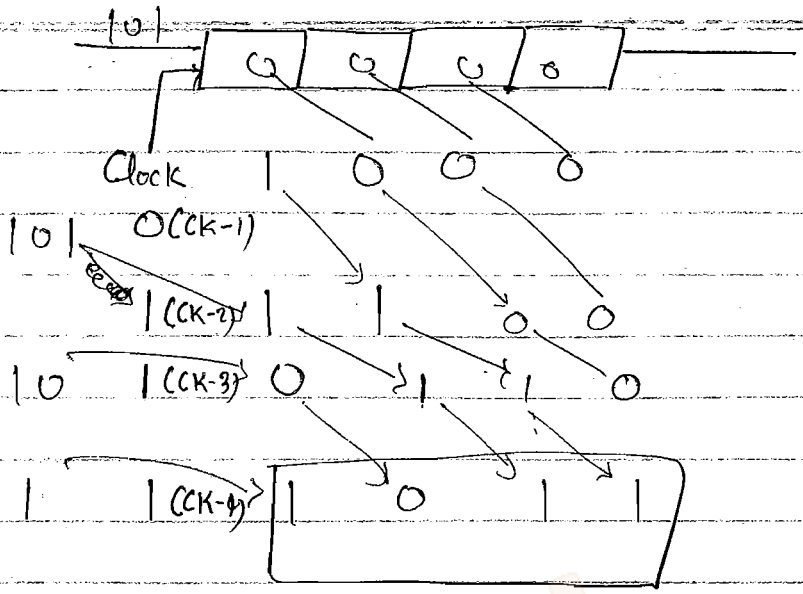
Based on input and Output Registors are Classified as -

1. Serial input Serial Output Register [SISO]
2. Serial input Parallel Output Register [SIPO]
3. Parallel input Parallel Output Register [PIPO]
4. Parallel input Serial Output Regrster [PISO]

1. Serial input Serial Output Registor [SISO] :- {4-bit SISO} :-

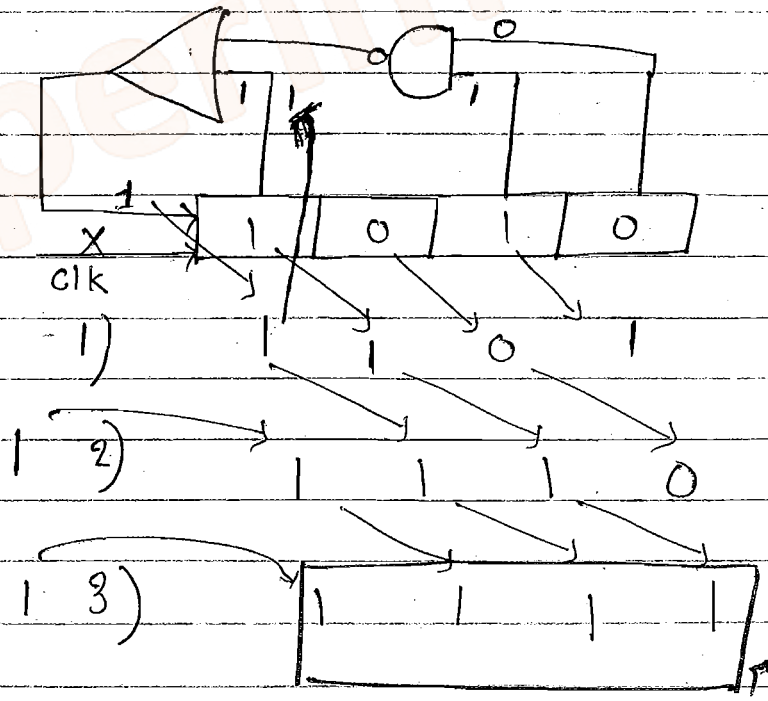






for n bit serial register for input storage n - clock pulse are required.

Ques For the given circuit diagram identify the content after three clock pulse.

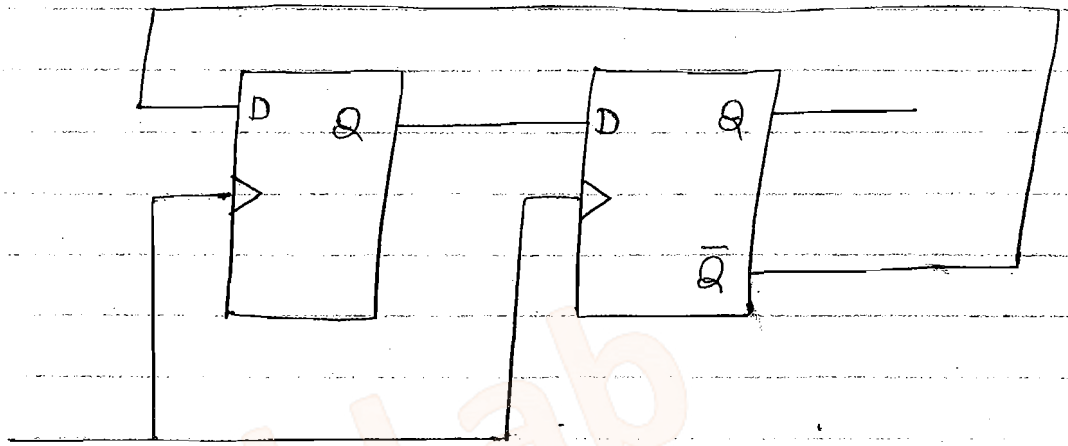


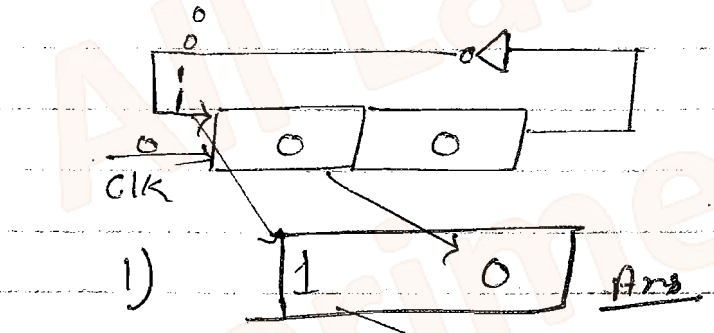
Soln

This the content after three clk pulses.

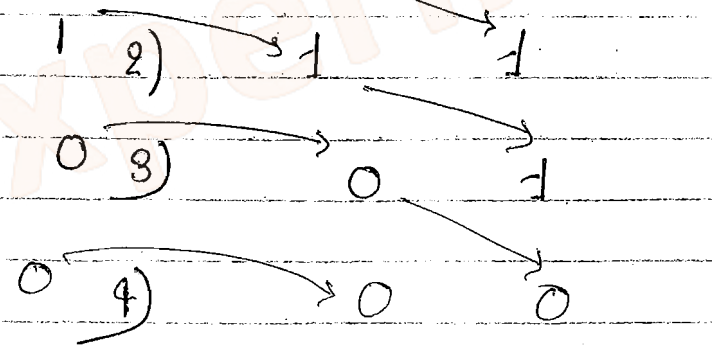
Ques for the given circuit diagram find the content after 333 clock pulse.

Sol^{n}





1) 1 0 Ans

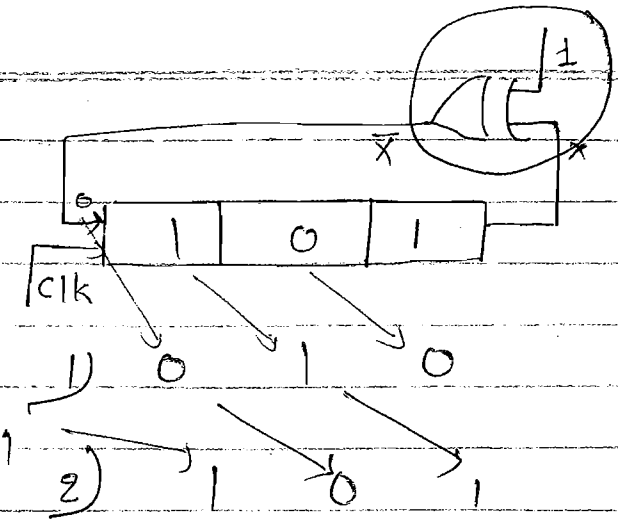


$$\begin{array}{r|l} & 83 \\ \hline 4 & 333 \\ & 32 \\ \hline & 13 \\ & 12 \\ \hline & 1 \end{array}$$

So after 83 clk we find 0 0 there for it mean previous state (1)
So after 333 clk pulse we find 10 as fist o/p.

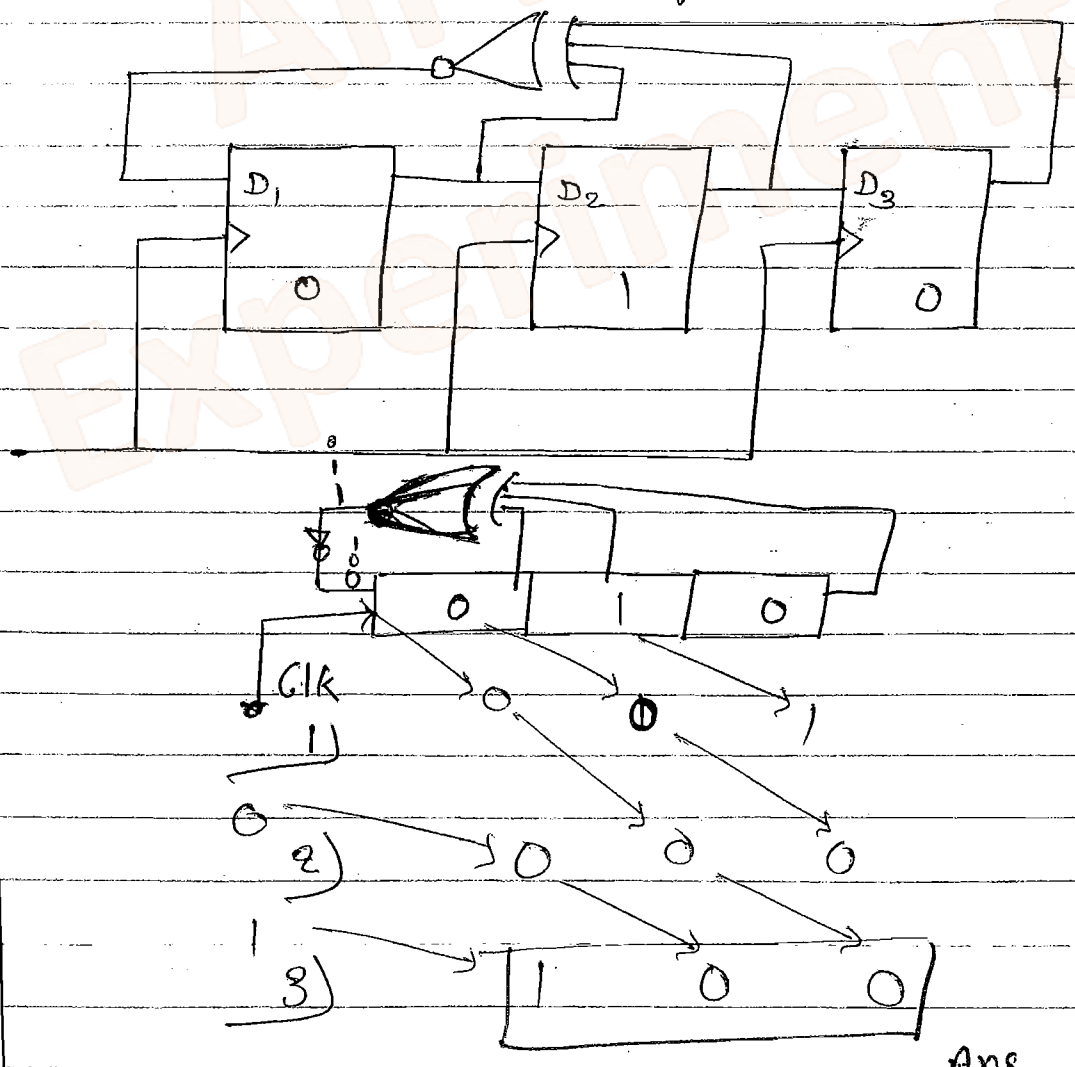
2. for the given circuit find the content after 332 clk pulse.

It is like a not gate.



So after two step we reach previous state so after 332 clk we get 101.

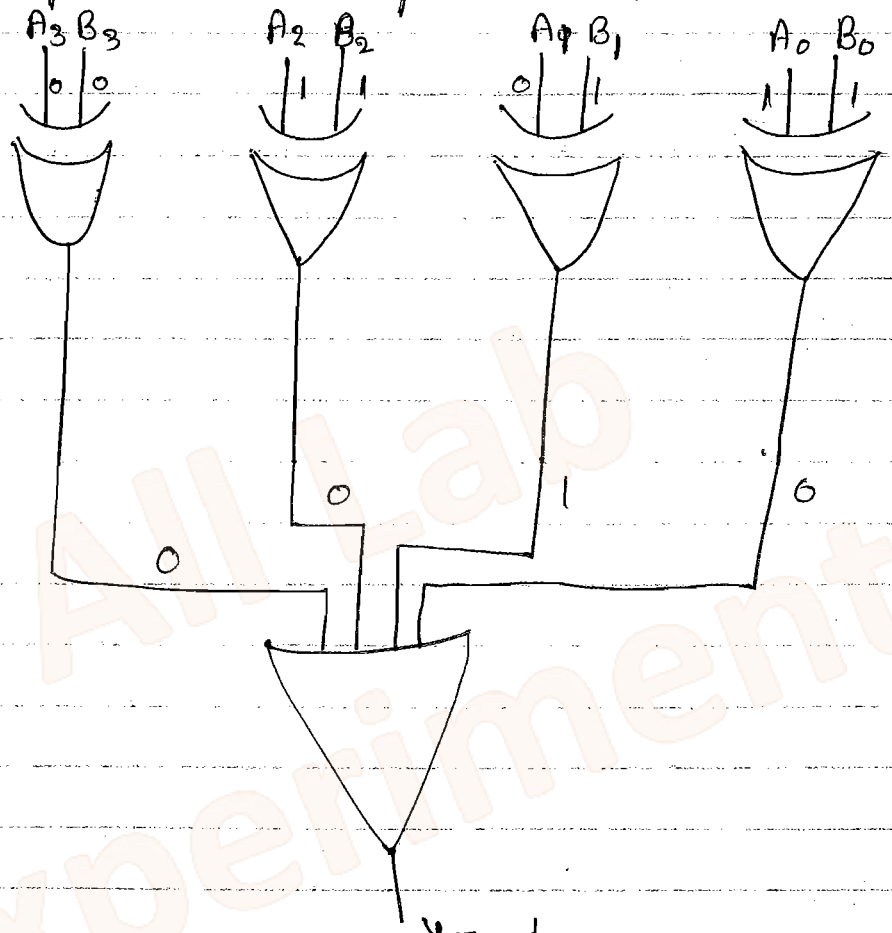
Q. Find the content after 3 clock pulse.



Ans

Qus for the given circuit diagram identify for which of the following combination of i/p produces high output.

Sol^n



	A_3 A_2 A_1 A_0	B_3 B_2 B_1 B_0
(a)	1 0 1 0	1 0 1 0
(b)	0 1 0 1	0 1 0 1
(c)	0 0 1 1	0 0 1 1
(d)	0 1 0 1	0 1 1 1 [✓]

Q. for the given circuit diagram determine the content after 3 clock pulse.

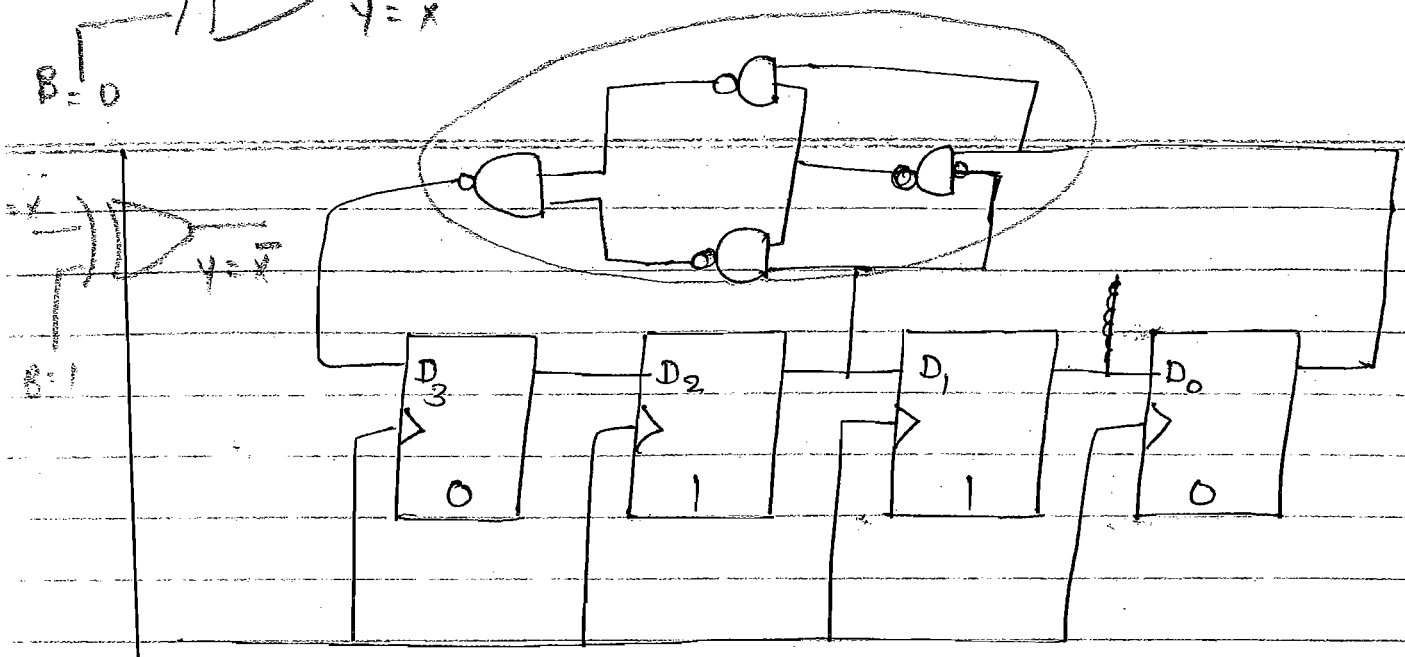
Sol^n

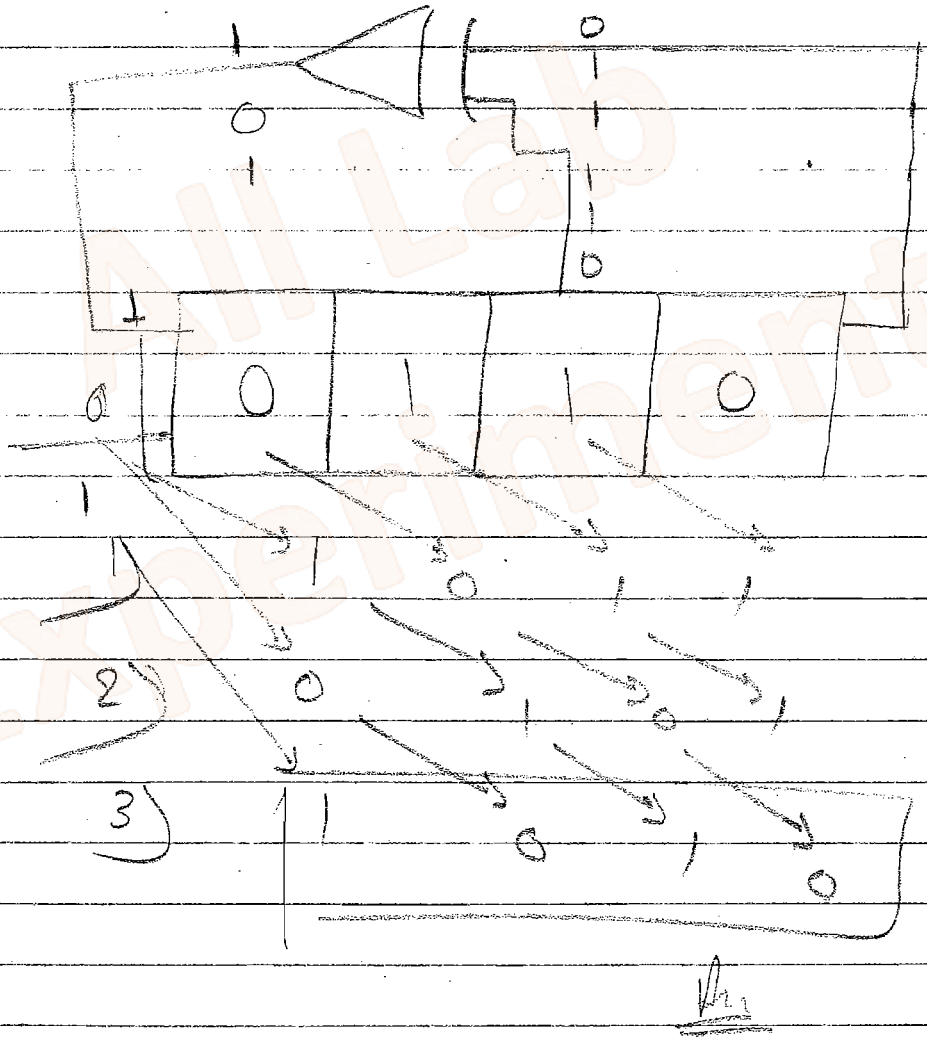
A = X

B = 0

Y = X

X-OR gate = $A\bar{B} + \bar{A}B = A \oplus B$





* **Counters :-**

These are used to count the number of clock pulses.

- These are used to measure the width (time period) of the clock pulse.
- These are used to measure the freequncy of clock pulse.
- These are used biomedical applicatim (ECG)
- These are used in the radar applicatim.
- These are used in the timer ll circuit.

Counters are basically classified as -

1. Assynchronous Counter [Slow]
2. Synchronous Counter [Fast]

* **Classification between Assynchronous and Synchroneus Counter :-**

Assynchroneus	Synchronous.
• In the assynchroneus counter only one flip-flop is applied by external clock pulse. Rest, every flip-flop having clock pulse applied by previous F.F.	• All the flip-flops are applied by same clock pulse.
• Delay is present (slow)	• Delay is not present (Fast.

• Decoding error present.	• No decoding error
• Only up (increasing ↑) or down (decreasing ↓) Count is possible	• Any count sequence is possible.
• It is also called as Ripple Counter.	• Ex - Ring / Johnson Counter.
• Only JK or T Flip-Flop is used.	• Any Flip-Flop is used

* ~~Asynchronous Counter~~

* **Modulus of a Counter :-**

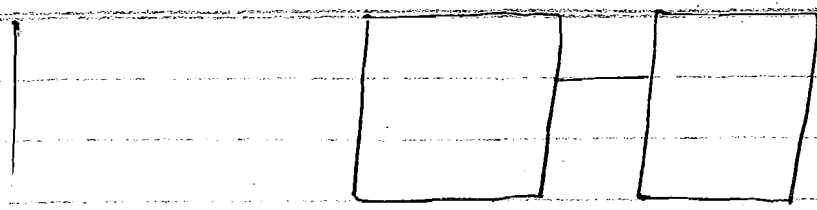
Mod of a counter represents number of state counted by counter.

over all mod = xyz

If the counters having mod x, mod y, mod z are cascated, then overall mod is xyz.

Qus A mod 78 counter can be implimented by -

(a) 6 number of mod 6 counter
(b) 13 number of mod 6 counter
(c) A mod 13 & a mod 6 counter [✓]
(d) 13 mod of mod 13 counter.



0 0
0 1
1 0
1 1

mod (4) → 2^2 ← no. of flip-flo

mod 8 :- 2^3 ← No. of flip-flop

mod 16 :- 2^4 ← No. of flip-flops.

no of mod → $N = 2^n$ → no. of flip-flops.

$\Rightarrow N = 2^n$

$\log N = \log 2^n$

$\log_2 N = n \log_2 2$

$$\boxed{n = \log_2 N} \quad \{\because \log_2 2 = 1\}$$

OR

$$\boxed{n \geq \log_2 N}$$

mod 8 = 3 flip flop

mod 7 = ? 3 flip-flo

2 = 4 (too less)

3 = 8