Analog system and applications
Semester 4
Solved Paper – 2018

Question Paper

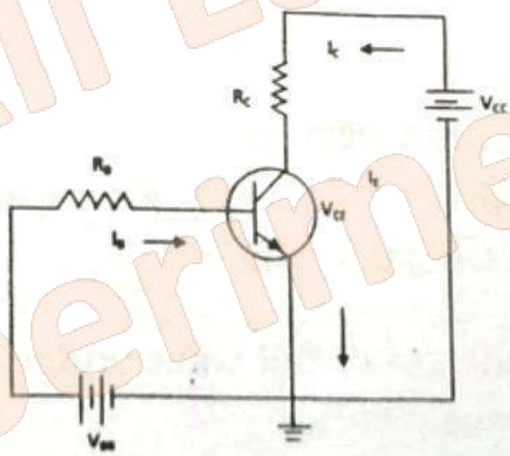
1. Attempt any **five** of the following:

(a) Define drift and diffusion currents in doped semiconductors.

(b) Explain with a circuit diagram, how Zener Diode is used in voltage regulation under varying load conditions.

(c) Draw the IV characteristics of a Solar cell for different intensities of light.

(d) Calculate the value of I_B, I_C and V_{CE} for the following circuit, given that R_B=470 kΩ; R_C = 2.2 kΩ; V_{BB}= V_{CC}= 18 V; β=100.

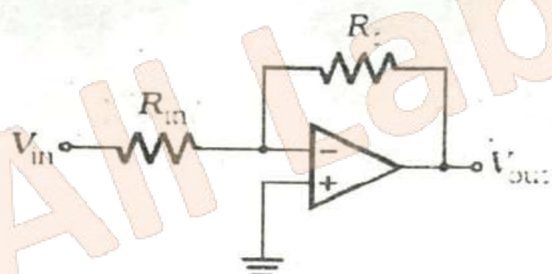


P. T. O.

(e) For a BJT compare the "voltage divider bias circuit" with the "fixed bias circuit" with respect to their stability.

(f) How does negative feedback, in an Amplifier, improve its stability?

(g) In the following circuit, open loop gain A of op-amp is 2×10^5 and $R_{in} = 1\ k\Omega$. Find the value of R_f if the resulting gain with feedback is to be 20 dB.



(h) Define accuracy and resolution for a D/A converter.

3x5=15

2. (a) Explain the formation of depletion region in a *p-n* junction. Derive an expression for the depletion width and barrier potential for *p-n* junction.

(b) A Germanium *p-n* step junction has donor density $N_d = 10^{17}\ cm^{-3}$ on *n* side and acceptor density $N_a = 10^{15}\ cm^{-3}$ on *p* side. Calculate the built-in potential at the junction if intrinsic carrier density $n_i = 10^{13}\ cm^{-3}$. Assume $kT/e = 0.026$ V.

10,5

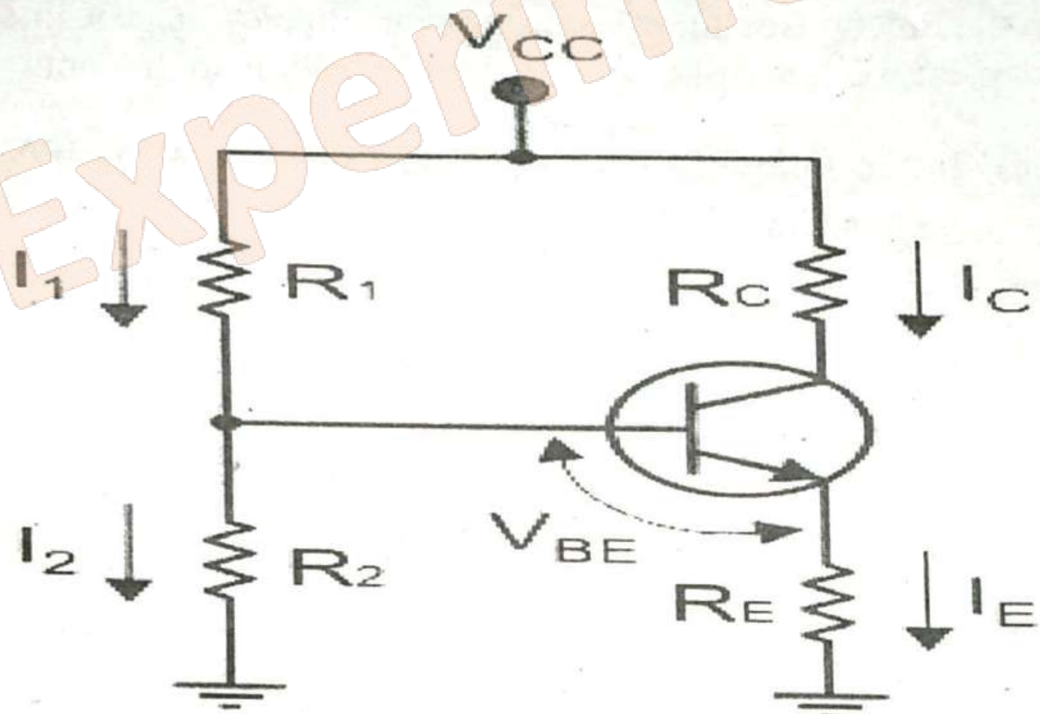
3. (a) Explain with a neat diagram the working of a full wave bridge rectifier. Derive the expression for its ripple factor and the rectification efficiency.

(b) Give advantages of full wave bridge rectifier over center tap full wave rectifier.

12,3

4. (a) Give the hybrid equivalent circuit of a CE Transistor. Derive the expressions for the current gain, input impedance and output admittance of a CE transistor amplifier using hybrid model.

(b) In the voltage divider bias circuit given below, V_{CC} =20 V, R_C =2 kΩ, R_E =3 kΩ, R_1= 10 kΩ and R_2 =6 kΩ. Draw the dc load line and determine the Q-point. 10, 5



5. Explain with a neat diagram RC coupled amplifier. Give its equivalent circuits in different frequency ranges. Obtain the expressions for its voltage gain in low and middle frequency regions. Sketch the frequency response curve.

15

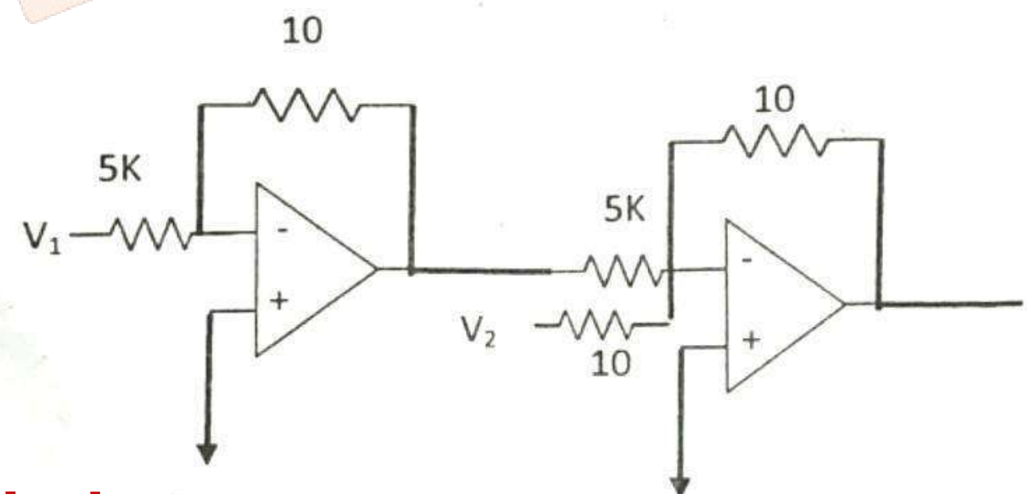
6. (a) Draw the circuit of a Colpitt Oscillator and explain its working. Derive the expressions for the frequency of oscillations, and the condition for sustained oscillations.

(b) In a phase shift oscillator, R= R_L =10 kΩ and C= 0.01 μF, calculate the time period of oscillation and h_{fe} of the transistor. 10, 5

7. (a) Draw the circuit of an Op-amp as a Differentiator and explain its operation.

(b) An op-amp integrator has R=1 MΩ and C=0.5 μF. With input signal 2 sin $100\pi t$ determine the output voltage as a function of time assuming that initial voltage across capacitor is zero. Sketch the output in relation to the input.

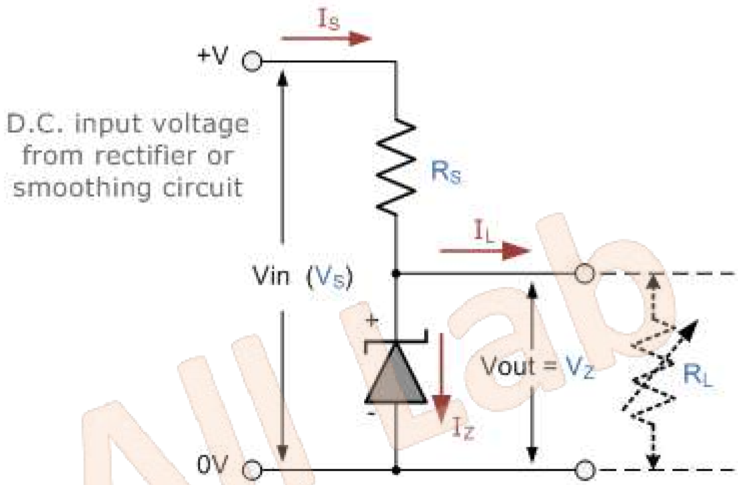
(c) In the following circuit calculate output voltage if V_1 =5 V and V_2 =2 V. 5,5,5



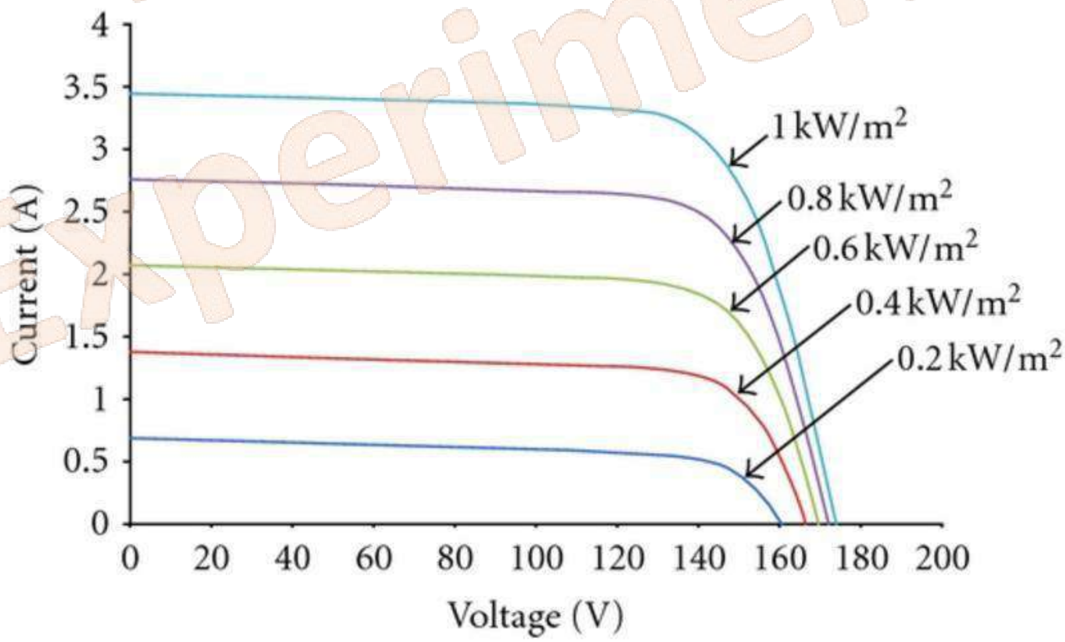
Solution

Ans 1a) Diffusion current is a current in a semiconductor caused by the diffusion of charge carriers (holes and/or electrons). This is the current which is due to the transport of charges occurring because of non-uniform concentration of charged particles in a semiconductor. The drift current, by contrast, is due to the motion of charge carriers due to the force exerted on them by an electric field. Diffusion current can be in the same or opposite direction of a drift current.

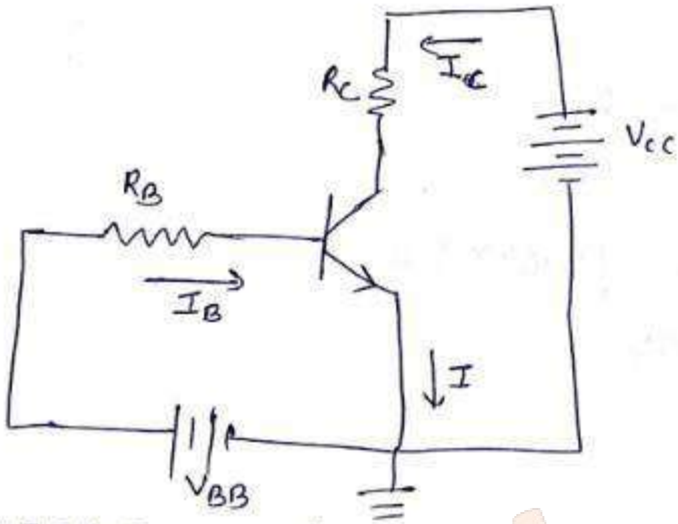
Ans 1b)



Ans 1c)



Ans 1d)



$R_B = 470\,K\Omega$ $\quad R_C = 2.2\,K\Omega$

$V_{BB} = 18V$ $\quad V_{CC} = 18V$ $\quad \beta = 100$

<u>In loop 1:</u>

$$-V_{BB} + I_B R_B + V_{BE} = 0 \quad — ①$$

<u>In loop 2</u>

$$-V_{CC} + I_C R_C + V_{CE} = 0 \quad — ②$$

for silicon transistor, $V_{BE} = 0.7V$

from equation ①

$$-18 + I_B(470\,K\Omega) + 0.7 = 0$$

$$I_B = \frac{18 - 0.7}{470}\ mA = \frac{17.3}{470} = 36.8\,\mu A$$

$$\beta = \frac{I_C}{I_B} \Rightarrow 100 \times 36.8 \times 10^{-6} = I_C$$

$$I_C = 3.68\,mA.$$

from equation 2

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 18 - [3.68 \times 2.2]$$

$$V_{CE} = 9.9V.$$

Ans 1e) refer your class notes

Ans 1f) The quantity that directly determines whether a negative-feedback circuit is stable or not is loop gain which is given by:

$$G_{CL} = \frac{A}{1 + A\beta}$$

This formula assumes that Aβ is a positive number (because positive Aβ means that the feedback is negative). What happens when Aβ is not positive? Consider the case when Aβ = -1:

$$G_{CL} = \frac{A}{1 + (-1)} = \frac{A}{0} = \infty$$

In this context, a closed-loop gain of infinity corresponds to an oscillator—even with zero input the output is saturated. Thus, the critical quantity in stability analysis is the loop gain.

Ans 1g) hint: use gain formula for inverting amplifier

Ans 1h) Accuracy can be defined as the amount of uncertainty in a measurement with respect to an absolute standard. Accuracy specifications usually contain the effect of errors due to gain and offset parameters. Offset errors can be given as a unit of measurement such as volts or ohms and are independent of the magnitude of the input signal being measured.

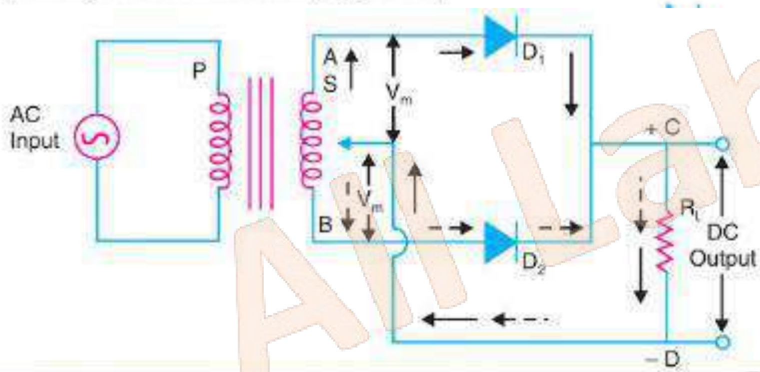
Resolution is the ratio between the maximum signal measured to the smallest part that can be resolved - usually with an analog-to-digital (A/D) converter.

It is the degree to which a change can be theoretically detected, usually expressed as a number of bits. This relates the number of bits of resolution to the actual voltage measurements.

Ans 2a) refer your class notes
Ans 2b) try yourself
Ans 3a)

In a full-wave rectifier both halves of the input-cycle are used. There are two types of full-wave rectifiers: (1) Centre tapped full-wave rectifier, and (2) Bridge rectifier.

Centre tapped full-wave rectifier. A full wave rectifier circuit consists of two diodes D_1 and D_2 connected to the secondary of the step-down transformer. The input A.C. signal is fed to the primary of the transformer (Fig. 58.15).



Working. During the positive half-cycle of the secondary voltage, one end of the secondary, say A, becomes positive and end B becomes negative. So the diode D_1 is forward biased, and diode D_2 is reverse biased. As a result of this, the diode D_1 conducts current whereas the diode D_2 does not conduct. Current through the load resistance flows from C to D producing output voltage V_0. The current is shown by solid arrows.

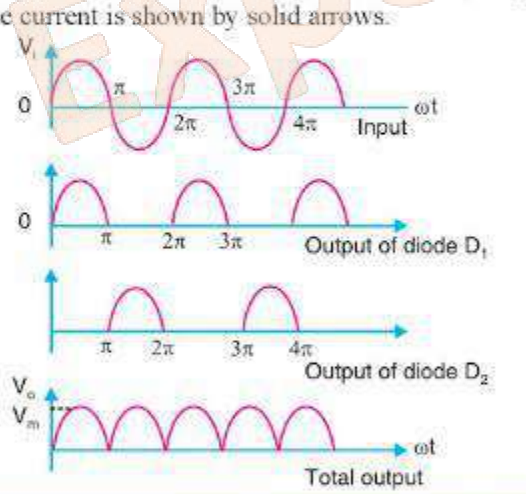


Fig. 58.16

Full-wave Rectifier

During the negative half cycle of AC input, end A becomes negative and end B positive. So the diode D_1 is reverse biased and the diode D_2 is forward biased. As a result, the diode D_1 does not conduct and D_2 conducts current. Again current flows from C to D through the load resistance R_L producing output voltage V_0. The current is shown by the dotted arrows.

Thus, during both the half cycles, current flows through the load in the same direction. The output voltage is developed across the load R_L during the entire cycle. It is a pulsating D.C. voltage containing both A.C. and D.C. components. The input and the rectified output wave-forms are shown in Fig. 58.16.

58.11 Mathematical Analysis

Let the diodes D_1 and D_2 be identical and have the same dynamic resistance R_f. At any instant, let the magnitudes of AC voltages applied to the diodes be each equal to $V_i = V_m \sin \omega t$. V_m is the peak input voltage.

Let R_f = dynamic forward resistance of the diode.

The current pulses in the two diodes are given by

$$i = \begin{Bmatrix} I_m \sin \omega t & \text{for } 0 < \omega t < \pi \\ -I_m \sin \omega t & \text{for } \pi < \omega t < 2\pi \end{Bmatrix} \quad ...(1)$$

Here, $$I_m = \frac{V_m}{R_f + R_L}.$$

(i) D.C. (average) value of output current. The output dc current I_{dc} is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i\, d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin \omega t\, d(\omega t) + \int_{\pi}^{2\pi} -I_m \sin \omega t\, d(\omega t)\right]$$

$$= \frac{I_m}{2\pi}\left[[-\cos \omega t]_0^{\pi} + [\cos \omega t]_{\pi}^{2\pi}\right] = \frac{I_m}{2\pi}[2+2]$$

$$\therefore \quad I_{dc} = \frac{2I_m}{\pi}. \quad ...(2)$$

(ii) R.M.S. (effective) value of load current. The r.m.s. value of total output current is given by

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2 d(\omega t)}$$

$$= \left[\frac{1}{2\pi}\left\{\int_0^{\pi} I_m^2 \sin^2 \omega t . d(\omega t) + \int_{\pi}^{2\pi} I_m^2 \sin^2 \omega t . d(\omega t)\right\}\right]^{1/2}$$

$$\therefore \quad I_{rms} = \frac{I_m}{\sqrt{2}}. \quad ...(3)$$

(iii) Power supplied to the circuit. The a.c. power input to the rectifier from the supply is given by

$$P_{\infty} = I_{rms}^2 (R_f + R_L) = \frac{(R_f + R_L) I_m^2}{2} \quad ...(4)$$

(iv) Average power supplied to the load R_L. The d.c. power output across the load R_L is given by

$$P_{dc} = I_{dc}^2 R_L = \frac{4 I_m^2 R_L}{\pi^2} \quad ...(5)$$

(v) Rectifier efficiency. In a rectifier, the useful power output is the d.c. power which is developed across the load R_L. Therefore, efficiency

$$\eta = \frac{\text{d.c. power supplied to the load}}{\text{Total input A.C. power}} \times 100\%$$

$$= \frac{P_{dc}}{P_{ac}} \times 100\% = \frac{4 I_m^2 R_L / \pi^2}{(R_f + R_L) I_m^2 / 2} \times 100\%$$

[Using Eqs. (4) and (5)]

$$\therefore \quad \eta = \frac{81.2}{1 + \dfrac{R_f}{R_L}} \% \quad ...(6)$$

Thus, the rectification efficiency of a full-wave rectifier is double that of a half-wave rectifier under identical conditions.

The maximum possible efficiency of a full-wave rectifier is 81.2 % when $R_f << R_L$.

(vi) Ripple factor. The ripple factor γ is given by

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_m / \sqrt{2}}{2 I_m / \pi}\right)^2 - 1}$$

$$\therefore \quad \gamma = \mathbf{0.482}$$

The ripple factor of a full-wave rectifier is 0.482 and is much smaller than that of half-wave rectifier. Hence, in actual practice, a full-wave rectifier is preferred to a half-wave rectifier.

Ans 3 b) Advantages of full wave rectifier as compared to centre tap full wave rectifier are as follows:

1:full wave rectifier has a complex circuit as compared to centre tap rectifier.

2: Four diodes are used in centre tap full wave rectifier so Voltage drop at diodes are twice of that center tapped rectifier.

Ans 4a)

Accordingly, the equivalent circuit is drawn in Fig. 62.2. Here the a.c. voltage source $h_{re} V_0$, which acts in opposition to the input signal V_i, represents the 'feedback' of the output voltage to the input circuit. The current source of magnitude $h_{fe} I_b$ may be looked as if the input current I_b is amplified and appears as $h_{fe} I_b$ in the output circuit. Thus $h_{fe} = \beta$, the current amplification factor.

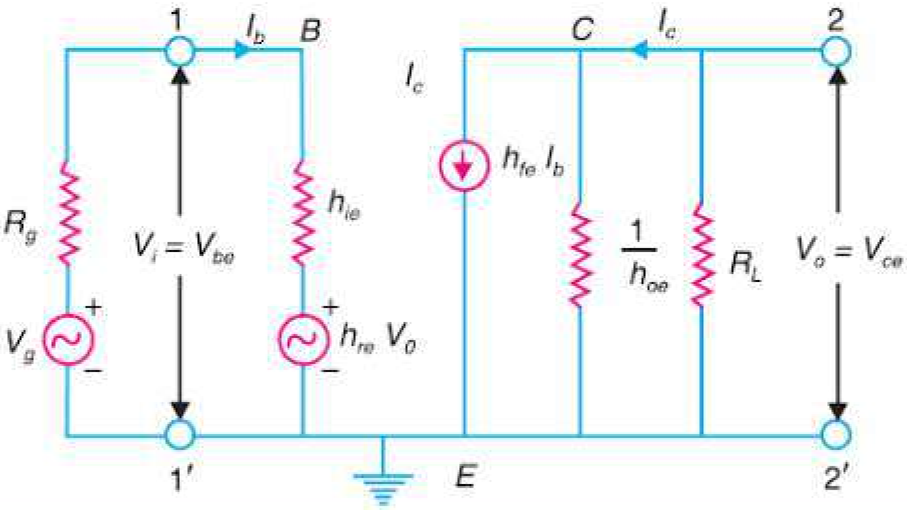


Fig. 62.2

(*i*) **Current Gain.** Let Z be the equivalent impedance of $1/h_{0e}$ and R_L in parallel. Then,

$$\frac{1}{Z} = 1/\frac{1}{h_{0e}} + \frac{1}{R_L} = h_{0e} + \frac{1}{R_L}$$

or

$$Z = \frac{R_L}{1 + h_{0e}\, R_L}$$

Voltage across R_L = voltage across Z

or

$$I_c\, R_L = h_{fe}\, I_b\, (Z) = h_{fe}\, I_b \left(\frac{R_L}{1 + h_{0e}\, R_L}\right)$$

or

$$\frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{0e}\, R_L}$$

$$\text{Current Gain } A_{ie} = \frac{\text{Output Current}}{\text{Input Current}}$$

$$\therefore \quad A_{ie} = \frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{0e}\, R_L}, \qquad ...(1)$$

(*ii*) **Input impedance.** The input impedance Z_{ie} of the transistor is the impedance at the input terminals 1 and 1′.

$$\text{Input impedance } Z_{ie} = \frac{\text{Input Voltage}}{\text{Input Current}} = \frac{V_i}{I_b}$$

But

$$V_i = h_{ie} I_b + h_{re} V_0$$

$$= h_{ie} I_b + h_{re}(-I_c R_L) \qquad (\because V_0 = -I_c R_L)$$

$$Z_{ie} = \frac{V_i}{I_b} = h_{ie} - h_{re} R_L \left(\frac{I_c}{I_b}\right)$$

∴

$$Z_{ie} = h_{ie} - h_{re} R_L A_{ie} = h_{ie} - \frac{h_{re} \cdot h_{fe} \cdot R_L}{(1 + h_{0e} \cdot R_L)} \qquad ...(2)$$

(*iii*) Voltage gai...

...output are 180° out of phase.

(*iv*) **Output impedance.** The output impedance Z_0 of an amplifier is defined as the ratio of the output voltage to the output current with the input signal generator V_g reduced to zero and replaced by its internal resistance R_g and an a.c. voltage source V_0 (rms) applied to the output terminals as shown in Fig. 62.3. Thus

$$Z_{0e} = \frac{V_0}{I_c}$$

where I_c is the current sent by the applied source.

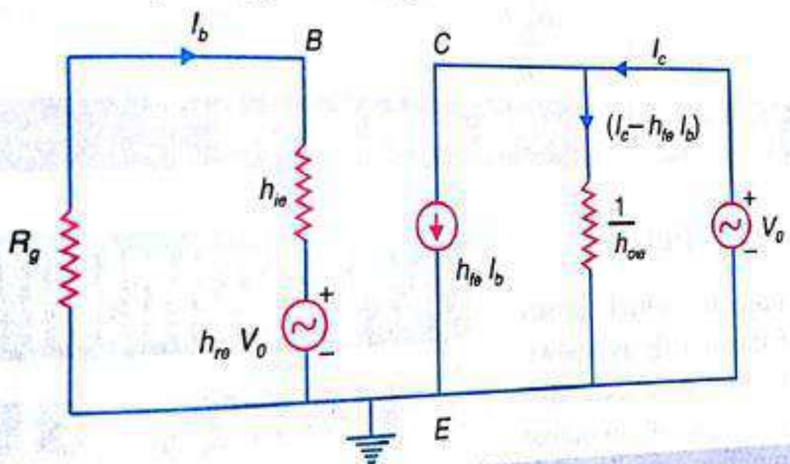


Fig. 62.3

Since the current through the output resistance $1/h_{0e}$ is $I_c - h_{fe} I_b$, the output voltage V_0 is given by

$$V_0 = (I_c - h_{fe} I_b)\frac{1}{h_{0e}}$$

or

$$h_{0e} V_0 = I_c - h_{fe} I_b$$

But the base current I_b is given by

$$I_b = -\frac{h_{re} V_0}{h_{ie} + R_g}$$

Substituting the value of I_b in Eq. (5), we get

$$h_{0e} V_0 = I_c + \frac{h_{fe} h_{re}}{h_{ie} + R_g} V_0$$

or

$$V_0\left(h_{0e} - \frac{h_{fe} h_{re}}{h_{ie} + R_g}\right) = I_c$$

or

$$Z_{0e} = \frac{V_0}{I_c} = \frac{1}{h_{0e} - \dfrac{h_{fe} h_{re}}{h_{ie} + R_g}}$$

$$\therefore \quad Z_{0e} = \frac{h_{ie} + R_g}{h_{0e}(h_{ie} + R_g) - h_{fe} h_{re}}$$

Ans 4b) solve it yourself.

Ans 5)

The cascaded amplifier where an *RC* network is used for interstage coupling is known as a resistance-capacitance (*RC*) coupled amplifier. A two-stage *RC* coupled transistor amplifier in the CE configuration is depicted in Fig. 9.2. The *coupling capacitor C* couples the output signal of the first stage to the input of the second stage. The capacitor blocks the dc voltage at the output of the first stage from appearing at the input of the second stage, but it allows the ac components of the output signal to pass through it. The quiescent operating point is determined by the supply voltage V_{CC} together with the resistances R_1, R_2, R_L and R_E. The *bypass capacitor* C_E in shunt with R_E has a very small reactance at the lowest signal frequency.

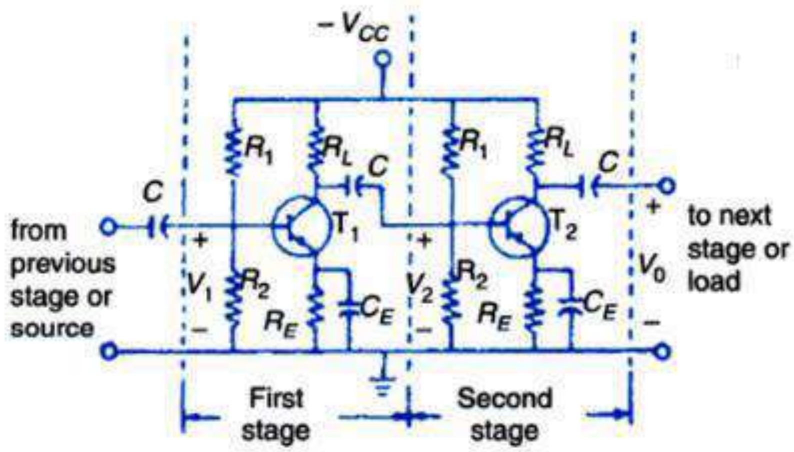


Fig. 9.2 A two-stage *RC*-coupled CE transistor amplifier.

The voltage gain of one stage, say the first stage, of the *RC*-coupled amplifier is

$$A_V = \frac{V_2}{V_1} = |A_V| \angle\theta. \tag{9.2}$$

The variation of the magnitude and the phase angle of the gain of an amplifier with frequency is referred to as the *frequency response characteristic* of the amplifier. A plot of the magnitude of the voltage gain $|A_V|$ with frequency for one stage of an *RC*-coupled amplifier is shown in Fig. 9.3. The plot of the phase angle θ of the voltage gain of the stage versus frequency is shown in Fig. 9.4. The frequency response characteristic of the stage has three regions: (*i*) the *mid-frequency range* where the voltage gain $|A_V|$ is approximately constant and the phase angle θ is 180° over a range of frequencies, (*ii*) the *low-frequency range* where the gain $|A_V|$ decreases and the phase angle increases over 180° with decreasing frequency below the mid-frequency range, and (*iii*) the *high-frequency range* where the gain $|A_V|$ falls off and the phase angle θ decreases below 180° with increasing frequency above the mid-frequency range.

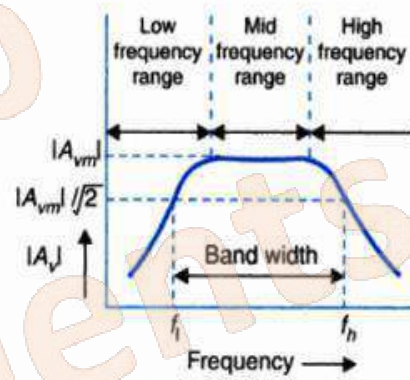


Fig. 9.3 $|A_v|$ versus frequency plot for one stage of an *RC*-coupled amplifier.

The fall of $|A_V|$ and the increase of θ over 180° with decreasing frequency in the low-frequency range are accounted for by the coupling capacitor *C*. As the reactance of a capacitor increases with diminishing frequency, the voltage drop across *C* becomes more important at low frequencies. The decrease of $|A_V|$ and the fall of θ below 180° in the high-frequency range are primarily determined by the transistor collector capacitance and the wiring capacitances appearing in shunt across the output. The drop of h_{fe} at high frequencies also contributes to the high-frequency response.

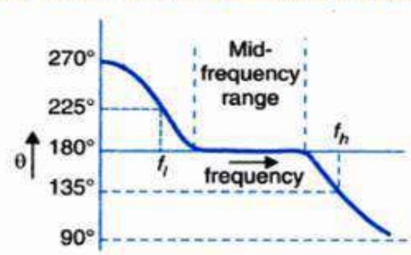


Fig. 9.4 θ versus frequency plot for one stage of an *RC*-coupled amplifier.

A. Mid-frequency Gain

In the mid-frequency range, the coupling capacitor C has a negligible reactance. Also, the output collector capacitor and other stray capacitors in shunt with the output are taken to be open-circuited. Replacing the transistor by its approximate hybrid model (see Sec. 8.9), we obtain the equivalent circuit of Fig. 9.5 for the first stage of the RC-coupled amplifier of Fig. 9.2.

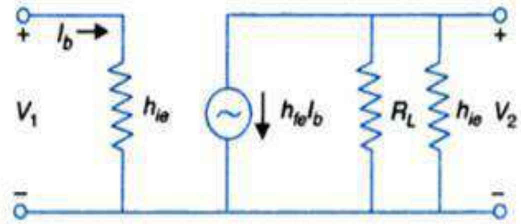


Fig. 9.5 Mid-frequency ac equivalent circuit of one stage of RC-coupled CE transistor amplifier.

The parallel combination of R_L and h_{ie} at the output gives the effective load resistance. R'_L That is,

$$\frac{1}{R'_L} = \frac{1}{R_L} + \frac{1}{h_{ie}} \quad \text{or} \quad R'_L = \frac{h_{ie}R_L}{h_{ie} + R_L} \tag{9.3}$$

The output voltage is

$$V_2 = -h_{fe} I_b R'_L \tag{9.4}$$

The input voltage is

$$V_1 = h_{ie} I_b \tag{9.5}$$

So, the mid-frequency voltage gain is

$$A_{Vm} = \frac{V_2}{V_1} = -\frac{h_{fe} R'_L}{h_{ie}} = -\frac{h_{fe} R_L}{h_{ie} + R_L} = -\frac{h_{fe}}{1 + (h_{ie}/R_L)} \tag{9.6}$$

The negative sign in Eq. (9.6) implies that the phase angle of the voltage gain is 180°. In other words, the output voltage leads the input voltage by 180°. Note that $|A_{Vm}|$ is independent of frequency and rises with R_L, approaching h_{fe} as $R_L \to \infty$.

B. Low-frequency Gain

In the low-frequency range, the reactance of the coupling capacitor C must be included. The shunt capacitor can, however, be considered to be an open-circuit. Thus the ac equivalent circuit of one stage of the RC-coupled amplifier below the mid-frequency range is as depicted in Fig. 9.6. Here the effective load impedance Z_L consists of the series combination of h_{ie} and C, shunted by R_L.

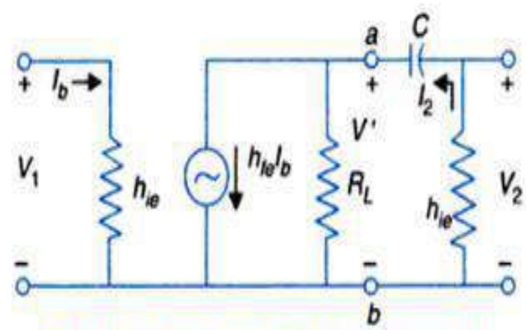


Fig. 9.6 Low-frequency ac equivalent circuit of one stage of RC-coupled CE transistor amplifier.

So,
$$\frac{1}{Z_L} = \frac{1}{R_L} + \frac{1}{h_{ie} - j/(\omega C)},$$

where ω (= $2\pi f$) is the angular frequency corresponding to the frequency f in the low-frequency range. Thus,

$$Z_L = \frac{h_{ie} - j/(\omega C)}{h_{ie} + R_L - j/(\omega C)} R_L \tag{9.7}$$

The voltage difference between the points a and b in Fig. 9.6 is

$$V' = -h_{fe} I_b Z_L. \tag{9.8}$$

If I_2 is the current through h_{ie} and C in series, we have

$$I_2 = -\frac{V'}{h_{ie} - j/(\omega C)} = \frac{h_{fe} I_b Z_L}{h_{ie} - j/(\omega C)}$$

The output voltage is

$$V_2 = -h_{ie} I_2 = -\frac{h_{ie} h_{fe} I_b Z_L}{h_{ie} - j/(\omega C)} \tag{9.9}$$

The input voltage is

$$V_1 = h_{ie} I_b. \tag{9.10}$$

From Eqs. (9.9) and (9.10), we have for the low-frequency voltage gain

$$A_{Vl} = \frac{V_2}{V_1} = -\frac{h_{fe} Z_L}{h_{ie} - j/(\omega C)} = -\frac{h_{fe} R_L}{h_{ie} + R_L - j/(\omega C)}, \tag{9.11}$$

where Eq. (9.7) is used. The magnitude and the phase angle of A_{Vl} are given by

$$|A_{Vl}| = \frac{h_{fe} R_L}{\sqrt{(h_{ie} + R_L)^2 + 1/(\omega^2 C^2)}} \tag{9.12}$$

$$\theta_l = 180^\circ + \tan^{-1} \frac{1}{\omega C(h_{ie} + R_L)} \tag{9.13}$$

From Eqs. (9.11) and (9.6), we obtain

$$A_{Vl} = \frac{A_{Vm}}{1 - j/[2\pi f C(h_{ie} + R_L)]} \tag{9.14}$$

Equation (9.14) relates the low-frequency voltage gain A_{Vl} to the mid-frequency voltage gain A_{Vm}. At the lower half-power frequency f_l, $|A_{Vl}| = |A_{Vm}|/\sqrt{2}$. So, Eq. (9.14) yields at $f = f_l$

$$\frac{|A_{Vm}|}{\sqrt{2}} = \frac{|A_{Vm}|}{\sqrt{1 + 1/[2\pi f_1 C(h_{ie} + R_L)]^2}}$$

or,

$$f_l = \frac{1}{2\pi C(h_{ie} + R_L)} \tag{9.15}$$

The low-frequency response improves, i.e. f_l is lowered when C and R_L are enhanced for a given transistor. Using Eq. (9.15), Eq. (9.14) can be written as

$$A_{Vl} = \frac{A_{Vm}}{1 - j(f_l/f)}, \tag{9.16}$$

so that $$|A_{Vl}| = \frac{|A_{Vm}|}{\sqrt{1+(f_l/f)^2}} \tag{9.17}$$

The phase angle by which A_{Vl} leads A_{Vm} is

$$\alpha_l = \tan^{-1}(f_l/f). \tag{9.18}$$

So the phase angle θ_l by which the output voltage V_2 leads the input voltage V_1 is

$$\theta_l = 180° + \tan^{-1}(f_l/f). \tag{9.19}$$

Equations (9.17) and (9.19) predict that $|A_{Vl}|$ drops and θ_l rises as f decreases. This behaviour is exhibited in Figs. 9.3 and 9.4. At $f = f_l$, we have from Eq. (9.19),

$$\theta_l = (180° + 45°) = 225°.$$

Ans 6a)

A Colpitts oscillator circuit is shown in Fig. 11.5(a). The dc operating point of the transistor in the active region of its characteristics is established by the resistors R_1, R_2, R_L, and R_E, and the supply voltage $-V_{cc}$. The capacitor C_B blocks the dc current flow from the collector to the base of the transistor through the coil of inductance L. The capacitor C_E is a bypass capacitor. The reactances of C_E and C_B are negligible at the frequency of oscillation. The inductance L and the capacitances C_1 and C_2 constitute the frequency-determining network.

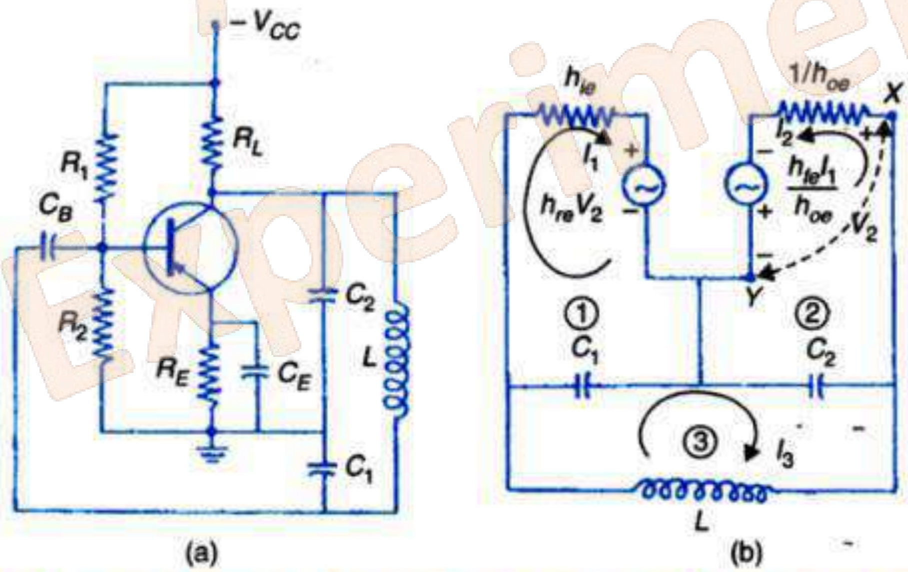


Fig. 11.5 (a) The circuit of a Colpitts oscillator, (b) Its AC equivalent circuit.

The transistor being in the CE configuration, introduces a phase shift of 180° between its input and output voltages. The voltage across the capacitor C_1, which is a fraction of the output voltage, is the feedback voltage. As the feedback voltage is 180° out of phase with the output voltage, the phase shift around the loop is 0° or 360°. It is noticed that Hartley and Colpitts oscillators are similar with the inductance and the capacitance interchanged.

Since R_1 and R_2 are large resistances, they do not affect the ac operation of the circuit. Also, R_E, being shunted by C_E which bypasses the ac, is excluded from the AC equivalent circuit, shown in Fig. 11.5 (*b*). Also, R_L is omitted since it is much larger than $1/h_{oe}$, and the current source is transformed into a voltage source in the AC equivalent circuit to facilitate the analysis.

The potential difference between the points *X*, *Y* in Fig. 11.5(*b*) is

$$V_2 = \frac{1}{h_{oe}} I_2 - \frac{h_{fe}}{h_{oe}} I_1 \tag{11.27}$$

Applying Kirchhoff's voltage law to loops (1), (2) and (3) in Fig. 11.5 (*b*), we obtain respectively

$$\left(h_{ie} - \frac{h_{fe}\, h_{re}}{h_{oe}} - \frac{j}{\omega C_1}\right) I_1 + \frac{h_{re}}{h_{oe}} I_2 + \frac{j}{\omega C_1} I_3 = 0 \tag{11.28}$$

$$-\frac{h_{fe}}{h_{oe}} I_1 + \left(\frac{1}{h_{oe}} - \frac{j}{\omega C_2}\right) I_2 - \frac{j}{\omega C_2} I_3 = 0 \tag{11.29}$$

and

$$\frac{j}{\omega C_1} I_1 - \frac{j}{\omega C_2} I_2 + j\left(\omega L - \frac{1}{\omega C_1} - \frac{1}{\omega C_2}\right) I_3 = 0. \tag{11.30}$$

where Eq. (11.27) has been used. At the angular frequency ω of oscillation, the tuned circuit is nearly resonant so that $\omega L - \frac{1}{\omega C_1} - \frac{1}{\omega C_2} = 0$, Assuming $h_{re} << 1$, and $h^2_{fe} >> 4\Delta_{he}$, the condition for the sustained oscillations and the frequency of oscillation can be derived in the same manner as for a Hartley oscillator. Thus, equating the real part of the determinant of the coefficients of I_1, I_2 and I_3 in Eqs. (11.28) through (11.30) to zero, we get

$$\frac{C_1}{C_2} \approx \frac{h_{fe}}{\Delta_{he}}, \tag{11.31}$$

where $\Delta_{he} = h_{ie}\, h_{oe} - h_{fe}\, h_{re}$. The *condition for sustained oscillations* in the Colpitts oscillator is given by Eq. (11.31). As $h_{fe} \approx 50$ and $\Delta_{he} \approx 0.5$, Eq. (11.31) shows that $C_1/C_2 \approx 100$.

Putting the imaginary part of the determinant of the coefficients of I_1, I_2 and I_3 in Eqs. (11.28) through (11.30) to zero, we get

$$\omega^2 = \frac{h_{oe}}{h_{ie}\, C_1 C_2} + \frac{1}{LC_1} + \frac{1}{LC_2} \tag{11.32}$$

The *frequency of oscillation* is

$$f = \frac{\omega}{2\pi} = \frac{1}{2\pi}\left(\frac{h_{oe}}{h_{ie}\, C_1 C_2} + \frac{1}{LC_1} + \frac{1}{LC_2}\right)^{1/2} \tag{11.33}$$

In practice, $h_{oe} / (h_{ie}\, C_1\, C_2) << [1/(LC_1) + 1/(LC_2)]$. Hence Eq. (11.33) reduces to

$$f \approx \frac{1}{2\pi\sqrt{LC_s}} \tag{11.34}$$

where $1/C_s = 1/C_1 + 1/C_2$. Clearly, C_s is the equivalent capacitance of C_1 and C_2 in series. Equation (10.34) shows that the frequency of oscillation is approximately the resonant frequency of the tank circuit.

Ans 6b)

$R = R_L = 10\,K\Omega, \quad C = 0.01\,\mu f$

Time period, $T = \dfrac{1}{C\sqrt{4RR_L + 6R^2}}$

$$= \frac{1}{0.01\times10^{-6}\sqrt{4(10\times10^3)^2 + 6(10\times10^3)^2}}$$

$$= \frac{1}{0.01\times10^{-6}\sqrt{10^9}} = 3.16\times10^{3}\ \text{sec}.$$

$$h_{fe} = 23 + 29\frac{R}{R_L} + 4\frac{R_L}{R}$$

$R = R_L$

$$h_{fe} = 23 + 29 + 4 = \underline{\underline{56}}$$

Ans 7a)

Fig. 65.8 (*a*) shows a circuit that performs the operation of differentiation.

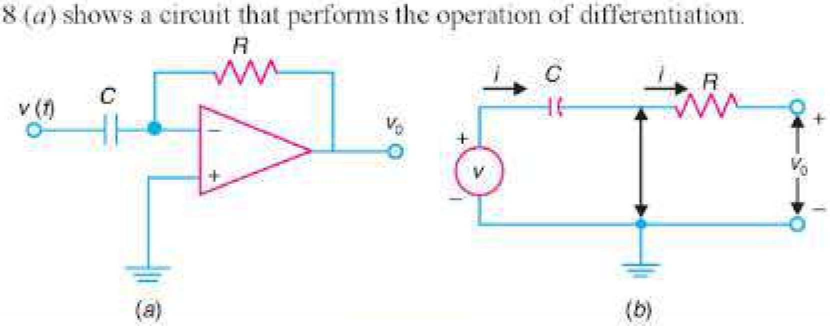


Fig. 65.8

The input signal source of voltage $v(t)$ is connected to the inverting input terminal through a capacitor C. The non-inverting input terminal is earth-connected. Negative feedback is given through a resistance R.

Let $v(t)$ be the signal voltage given as the input, which drives varying current through the capacitance C.

We see from the equivalent circuit of Fig. 65.8 (b) that

$$i = C\frac{dv(t)}{dt} \quad ...(1)$$

$$v_0 = -Ri = -RC\frac{d}{dt}v(t) \quad ...(2)$$

Hence, the output voltage is proportional to the differential of the input voltage.

Ans 7b) : try yourself