

Name of Paper : Digital Systems and Applications
Name of the Course : B.Sc. (Hons.) Physics (CBCS)
Semester : III
Duration : 3 Hours
Maximum Marks : 75

2021

Attempt any four questions.
All questions carry equal marks.

Q. 1. (a) Draw a neat and labeled block diagram of a cathode ray oscilloscope (CRO). Explain how a CRO is used to estimate the frequency, time period, phase and voltage of a sinusoidal waveform.

Sol. See Q. 1. [Page No. 149].

(b) Find X for the following numbers :

(i) $(AEF7.2E)_{16} = (X)_8$

(ii) $(25.75)_8 = (X)_{BCD}$

Sol. (i) $(AEF7.2E)_{16} = (X)_8$

In hexadecimal number,

A → 1010 2 → 0010

E → 1110 E → 1110

F → 1111

7 → 0111

For octa conversion, make the grouping of 3.

$$\begin{array}{cccccccc}
 \underline{001} & \underline{010} & \underline{111} & \underline{011} & \underline{110} & \underline{111} & \underline{001} & \underline{011} & \underline{100} \\
 \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\
 1 & 2 & 7 & 3 & 6 & 7 & 1 & 3 & 4
 \end{array}$$

$(X)_8 = (127367.134)_8$

(ii) $(25.75)_8 = (X)_{BCD}$

First convert octa to decimal

$$2 \times 8^1 + 5 \times 8^0 + 7 \times 8^{-1} + 5 \times 8^{-2}$$

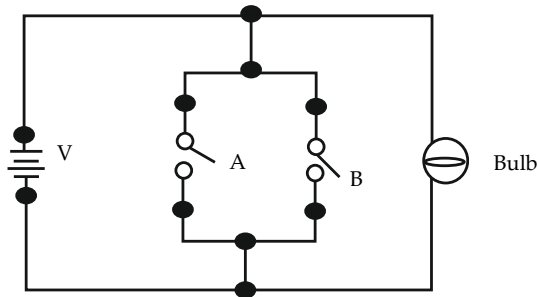
$(21.953)_{10}$

$(21)_{10} = (00100001)_{BCD}$

$(0.953)_{10} = (1111)_{BCD}$

$(25.75)_8 = (00100001.1111)_{BCD}$

OFF (0) and will cause the bulb ON(1) or OFF (0) :



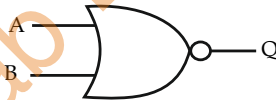
(i) Determine all the possible conditions of the switches for the bulb to be ON(1) and OFF(0) and tabulate it in the form of a truth table.

(ii) Name the logic operation performed by the circuit.

(iii) Draw the logic symbol of the circuit.

Sol.	A	B	Bulb	
	OFF	OFF	ON	
	OFF	ON	OFF	Short Circuit – all current will pass through B
	ON	OFF	OFF	Similar reason
	ON	ON	OFF	Similar reason

This is like NOR gate.



Q. 2. (a) Simplify the following expressions using Boolean Algebra :

(i) $(\overline{A}\overline{B} + \overline{A}\overline{C})(BC + \overline{B}\overline{C})(AB)$

(ii) $\overline{\overline{AB} + ABC + A(B + \overline{AB})}$

Sol. (i) $(\overline{A}\overline{B} + \overline{A}\overline{C})(BC + \overline{B}\overline{C})(AB)$

$$A(\overline{B} + \overline{C}) B (C + \overline{C})(AB)$$

Using A. $A = A$ B. $B = B$, we get

Now $C + \overline{C} = 1$

$\therefore AB(\overline{B} + \overline{C}) = AB\overline{B} + ABC\overline{C}$

$$= 0 + ABC$$

$$\{BB = 0\}$$

$$= ABC$$

$$(ii) \overline{\overline{AB} + ABC + (A(B + \overline{AB}))}$$

$$(A\overline{B} + ABC) \overline{(A(B + \overline{AB}))}$$

$$\left\{ \begin{array}{l} \text{Using } \overline{AB} = \overline{A} + \overline{B} \\ \overline{A + B} = \overline{A} \overline{B} \end{array} \right\}$$

$$A(\overline{B} + BC)(\overline{A} + \overline{(B + \overline{AB})})$$

$$A(\overline{B} + BC)(\overline{A} + \overline{B})(\overline{A\overline{B}})$$

$$A(\overline{B} + BC)(\overline{A} + \overline{B})(\overline{A} + B)$$

$$A(\overline{B} + BC)(\overline{A} + \overline{A}\overline{B} + 0)$$

$$A\overline{A}(\overline{B} + BC) + A\overline{A}\overline{B}(\overline{B} + BC)$$

$$\text{Since } A\overline{A} = 0$$

$$\therefore = 0$$

(b) Minimize the following expression using K-map method :

$$F(A, B, C, D) = \sum m(1, 3, 7, 8, 9, 11, 13, 15) + d(0, 2, 10, 14)$$

$$\text{Sol. } F(A, B, C, D) = \sum m(1, 3, 7, 8, 9, 11, 13, 15) + d(0, 2, 10, 14)$$

$$F = AD + CD + \overline{B}$$

$$= D(A + C) + \overline{B}$$

	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	X	1	1	X
$\overline{A}B$			1	
AB		1	1	X
$A\overline{B}$	1	1	1	X

(c) Implement the following expression using 8×1 multiplexer:

$$F(A, B, C) = \overline{A}C + \overline{B}C + ABC$$

Sol.

$$F(A, B, C) = \bar{A}C + BC + ABC$$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}		1	1	
A		1		1

$$F(A, B, C) = \sum m(1, 3, 5, 6)$$

Q. 3. (a) Write the sign magnitude form and 2's complement form for the following decimal numbers :

(i) + 10

(ii) - 14

Sol. + 10

- 14

Sign magnitude - 00001010

Sign magnitude - 10001110

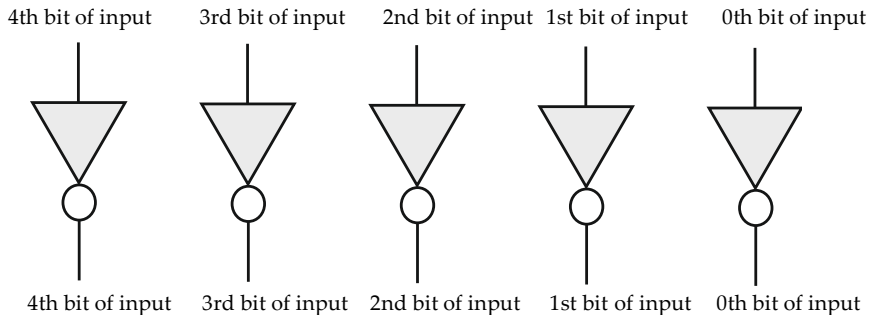
2's Complement - 11110110

2's Complement - 11110010

(b) Draw and explain the circuit diagram to find the 1's complement and 2's complement of a 4-bit number.

Sol. 1's complement : In number representation techniques, the binary number system is the most used representation technique in digital electronics. The complement is used for representing the negative decimal number in binary form. Different types of complement are possible of the binary number, but 1's and 2's complements are mostly used for binary numbers. We can find the 1's complement of the binary number by simply inverting the given number. For example, 1's complement of binary number 1011001 is 0100110. We can find the 2's complement of the binary number by changing each bit(0 to 1 and 1 to 0) and adding 1 to the least significant bit. For example, 2's complement of binary number 1011001 is (0100110)+1=0100111.

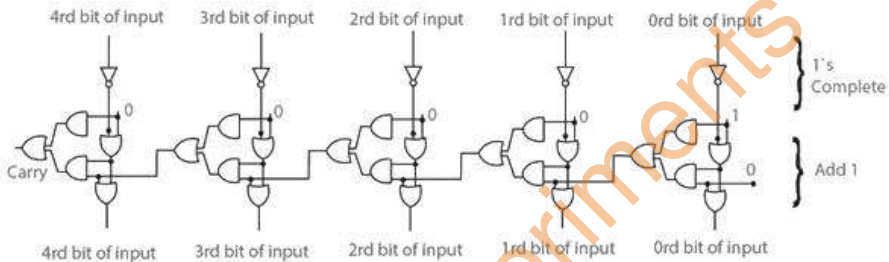
For finding 1's complement of the binary number, we can implement the logic circuit also by using NOT gate. We use NOT gate for each bit of the binary number. So, if we want to implement the logic circuit for 5-bit 1's complement, five NOT gates will be used.



For finding 1's complement of the given number, change all 0's to 1 and all 1's to 0. So the 1's complement of the number 11010.1101 comes out **00101.0010**.

2's complement : Just like 1's complement, 2's complement is also used to represent the signed binary numbers. For finding 2's complement of the binary number, we will first find the 1's complement of the binary number and then add 1 to the least significant bit of it.

For example, if we want to calculate the 2's complement of the number 1011001, then firstly, we find the 1's complement of the number that is 0100110 and add 1 to the LSB. So, by adding 1 to the LSB, the number will be $(0100110)+1=0100111$. We can also create the logic circuit using OR, AND, and NOT gates. The logic circuit for finding 2's complement of the 5-bit binary number is as follows:



Example 1 : 110100

For finding 2's complement of the given number, change all 0's to 1 and all 1's to 0. So the 1's complement of the number 110100 is 001011. Now add 1 to the LSB of this number, i.e., $(001011) + 1 = 001100$.

(c) Draw a circuit diagram of clocked JK flip-flop using NAND gates only. Explain its working and give its truth table. Explain the race around condition and its consequences?

Sol. See Q. 3. [Page 181].

Q. 4. (a) Draw a pin-out diagram of a 555 timer IC. Give any two applications of 555 timer IC.

Sol. See Q. 6. [Page 186].

(b) The content of a 4-bit SISO shift register is initially 1011. The data is shifted 7 times, one bit at a time, to right with the serial input being $1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 1 \rightarrow 0$. Write the contents of the shift register after each shift.

Sol. Initial data 1011.

Serial input being shifted to right $1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 1 \rightarrow 0$

Ist Cycle – 0101

IInd Cycle – 1010

IIIrd Cycle – 1101

IV Cycle – 0110

V Cycle – 1011

(c) Draw the circuit diagram of a MOD – 5 synchronous UP counter using JK flip-flop.

Sol. Synchronous Counters: It means that all flip-flops are clocked concurrently. The clock pulses drive the clock input of each flip-flop together hence there is no propagation delay.

Mod-5 Counter Synchronous Counter: This have five counter states. The counter design table for such counter shows the three flip-flop and their states also (0 to 5 states), as in table (a), the 6 inputs needed for the three flip-flops. The flip-flop inputs needed to step up the counter from the current to the next state have been worked out along with the assist of the excitation table illustrated in the table.

Inputs pulse	Counter States			Flip-Flop Inputs				
	A	B	C	JA KA	Y	JB JC	KB KC	
0	0	0	0	1	X	0	X	0
1	1	0	0	X	1	1 X	X	0
2	0	1	0	1	X	X X	0	0
3	1	1	0	X	1	X X	1	1
4	0	0	1	0	X	0 1	X	X
5(0)	0	0	0					

Table (a) counter Design Table for Mod-5 Counter

A flip-flop: The first state is 0. This change to 1 after the clock pulses. Thus JA must be 1 and KA may be 0 or 1 (i.e. X).

B flip-flop: The first state is 0 and this keeps unchanged after the clock pulse. Thus JB must be 0 and KB may be 0 or 1 (i.e. X)

C flip-flop: The state keeps unchanged. Thus Jc must be 0 and KC must be X. The flip-flop input values are entered in Karnaugh maps demonstrated in Table (b) [(i) (ii) (iii) (iv) (v) and (vi)] and a boolean expression is determined for the inputs to the 3-flip-flops and after that each expression is simplified. All the counter states have not been utilized; X's (don't) are entered to indicate un-utilized states. For each input the simplified expressions demonstrated under each map. At last,

diagram for the counter that is demonstrated in fig. (b).

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	1	0	X	1
A	X	X	X	X

(i) Map for J_A

$$J_A = \bar{C}$$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	0	0	X	X
A	1	X	X	X

(iii) Map for J_B

$$J_B = A$$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	0	X	X	0
A	0	X	X	1

(iii) Map for J_C

$$J_C = AB$$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	X	X	X	X
A	1	X	X	1

(ii) Map for K_A

$$K_A = 1$$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	X	X	X	0
A	X	X	X	1

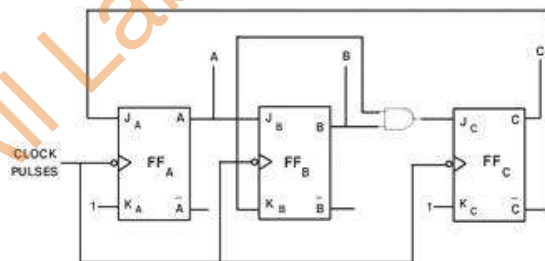
(iv) Map for K_B

$$K_B = A$$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	X	1	X	X
A	X	1	X	1

(iv) Map for K_C

$$K_C = 1$$



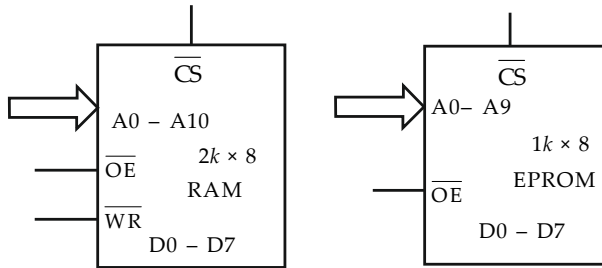
Q. 5. (a) What do you mean by volatile and non-volatile memories? List the various types of volatile and non-volatile memories.

Sol. See Q. 1. [Page 197].

(b) Draw the memory interfacing circuit diagram of 8085 microprocessor based system consisting of one ROM chip of 8 KB and two RAM's of 4KB each. Write the address ranges for each chip.

Sol. The first step to solve this problem is to understand the pins of the given memory chips.

RAM and ROM both have same pins, except for WR pin, which is present in RAM and is not there in a ROM. Let us understand the pins one by one.

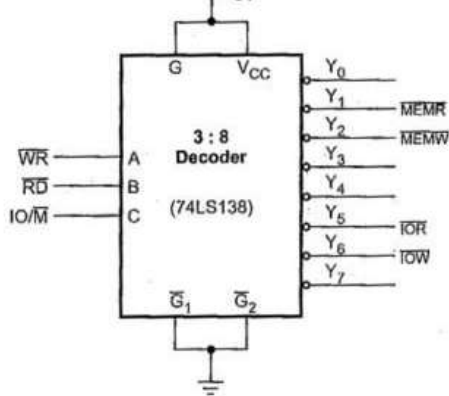


- **Data pins :** Since each memory location stores eight bits, there are eight data lines D0-D7 connected to the memory chip.
- **Address pins :** The number of address pins depends on the size of the memory. In this case, a memory of size 1 kB x 8 will have 2^{10} different memory locations. Hence, it will have ten address lines A0 to A9. Similarly, the 2 kB RAM will have 2^{11} different memory locations. So, there are 11 address lines A0-A10.
- **CS pin :** When this pin is enabled, the memory chip knows that the microprocessor is talking to it and responds to it accordingly. We need to generate this signal for each of the chips according to the range of addresses assigned to them. Basically, we select a chip only when it is needed. The Chip Select (CS) pin is used for this.
- **OE pin :** When this active-low output enable pin is enabled, the memory chip can output the data into the data bus.
- **WR pin :** Upon activation of this active-low memory write pin, data on the data bus is written on the memory chip at the location specified by the address bus.
- **VCC and GND pins :** These pins serve the purpose of powering the ICs. For simplicity, we will not show these pins in the diagram.

There are three types of buses in 8085 – Address bus, data bus, and control bus. Each of these buses will be connected to the memory chip.

Connecting Control Signals

In the memory chips, there are two pins for control signals – OE (Output Enable) and WR (Memory Write). These will be connected to the **control signals generated using a 3 to 8 decoder**. To read about the generation of control signals, you can read our post on Demultiplexing of Bus and Generating Control Signals. The circuit for generating control signals is shown below.



Four control signals are generated when we input the WR, RD and IO/M signals from the 8085 to the 3:8 decoder – IOR, IOW, MEMR and MEMW. Since we are dealing with memory, we will just need MEMR and MEMW signals.

While reading from a memory chip, its output should be enabled. So, MEMR will be connected to the OE pin. Similarly, for writing to a memory chip, MEMW will be connected to the WR pin of the RAM. After completing these two connections, we are done with the control signals except CS. We will deal with that in a bit.

(c) Write an assembly language program to subtract 2CH from C2H which are stored in memory locations 2000H and 2001H respectively using direct addressing mode. Store the result in the memory location 2002H and borrow in 2003H. What will be the contents of memory locations 2002H and 2003H after the execution of program?

Sol. Given 2000H – C2H
 2001H – 2CH
 2002H – Result
 2003H – Borrow

Program memories of sub. by direct addressing mode

```

MOV C, A
LDA, 2000H
MOV B, A
LDA, 2001H
SUB B
STA, 2002H
JNC, 2013H
INRC
MOV A, C
STA, 2003H

```

Content of memory 2002H – 96H

Content of memory 2003H – 01H

Q. 6. (a) Draw and explain the logic circuit for the generation of control signals of microprocessor 8085.

Sol. See Q. 1. [Page 202].

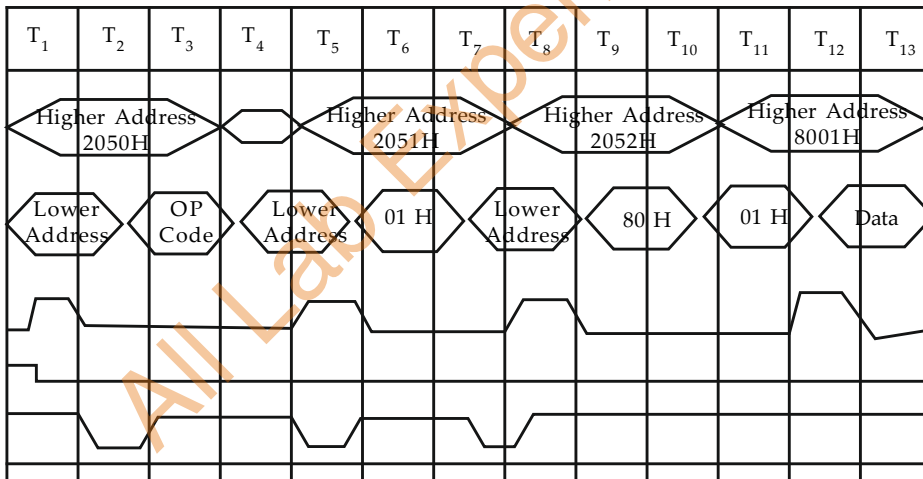
(b) What happens to the microprocessor 8085 when $\overline{\text{RESET IN}}$ pin is asserted low?

Sol. 1. The program counter is set to zero 2. The buses are tristated 3. The MPU is reset.

(c) Draw and explain the timing diagram of the following instruction :

2000H	LDA 2050H	3AH
2001H		50H
2002H		20H

Determine the time required for the execution of the instruction if the clock frequency is 3 MHz.



Note : Timing diagram of STA LDA are exactly the same in LDA.



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