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Q. 1. Answer any five of the following : 5 ×3

(a) Subtract decimal number 12 from decimal 9 using two's complement notation.

Ans. Consult yourbook.

(b) Describe with an example each of 1 -Byte, 2-Byte and 3-Byte instructions in 8085 microprocessor.

Ans. Consult yourbook.

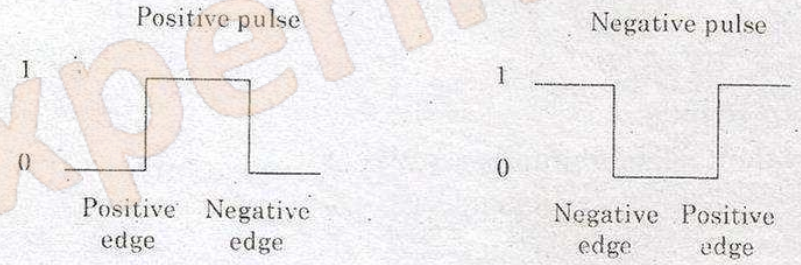
(c) The accumulator of 8085 microprocessor contains 5CH and carry is set. What will the accumulator contain and carry contain following each instruction given below

(i) XRA A **(ii)RAL**

Ans. Consult yourbook.

(d) What is meant by the term edge clocked/triggered and draw a digital symbol of a negative edge triggered JK flip flop.

Ans. Clock Pulse Transition. The movement of a trigger pulse is always from a 0 to 1 and then 1 to 0 of a signal. Thus is takes two transitions in a single signal. When it moves from 0 to 1 it is called a positive transition and when it moves from 1 to 0 it is called a negative transition. To understand more take a look at the images below :



Definition of clock pulse transition

Clock Pulse Transition. The clocked flip-flops already introduced are triggered during the 0 to 1 transition of the pulse, and the state transition starts as soon as the pulse reaches the HIGH level. If the other inputs change while the clock is still 1, a new output state may occur. if the flip-flop is made to then the multiple-transition problem can be eliminated.

The muliti-transition problem can be stopped is the flip flop is made to

respond to the positive or negative edge transition only, other than responding to the entire pulse duration.

(e) Convert the hexadecimal number $8AD9_{16}$ to its octal equivalent.

Ans. $(8AD9)_{16} = (?)_8$

First change this number to its equivalent decimal number:

$$8 \times 16^3 + 10 \times 16^2 + 13 \times 16^1 + 9 \times 16^0$$

$$32768 + 2560 + 208 + 9$$

$$(35545)_{10}$$

Now change this decimal number to octal:

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8	35545	
8	4443	1
8	555	3
8	69	3
8	8	5
	1	0

$(105331)_8$

So, $(8AD9)_{16} = (105331)_8$

(f) What is the largest decimal value that can be represented in binary using?

(i) one byte and (ii) two byte

Ans. (i) One Byte

One Byte means 8 bits.

Highest equivalent decimal number

$$= 2^8 - 1$$
$$= 256 - 1$$
$$= 255$$

(ii) Two Bytes

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This is equal to 16 bits

Highest equivalent decimal number $= 2^{16} - 1$

$$= 65536 - 1$$
$$= 65535$$

(g) Explain rise time, fall time and duty cycle of a square wave.

Ans. Rise Time (t_r)

It is the time taken by the output voltage (or current) to rise from 10% to 90% of its maximum value.

It primarily depends on diffusion capacitance C_D of the transistor.

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Fall Time (t_f)

It is the time interval during which the output voltage (or current) falls from 90% of its maximum value to 10%

Duty Cycle

It is defined as

$$D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

Where R_A and R_B are the resistances through which the capacitor is charged please ref. Q. 5 (a) also.

(h) Prove the following Boolean equations:

(i) (A + B) (A + $\bar{B}$) ($\bar{A}$ + C) = AC

(ii) ABC + A$\bar{B}$C + AB$\bar{C}$ = A(B + C)

Ans. (i) $(A + B)(A + \bar{B})(\bar{A} + C) = AC$

Let $y = (A + B)(A + \bar{B})(\bar{A} + C) = (AA + A\bar{B}) + (BA + B\bar{B})(\bar{A} + C)$

$= (A + A\bar{B} + A\bar{B})(\bar{A} + C)$ $\quad [\because B\bar{B} = 0]$

$= \left[A(1 + B) + A\bar{B}\right](\bar{A} + C)$

$= (A + A\bar{B})(\bar{A} + C)$

$= A(1 + B)(\bar{A} + C)$

$= (A \cdot 1)(\bar{A} + C)$

$= A(\bar{A} + C)$

$= A\bar{A} + AC$ $\quad \because A\bar{A} = 0$

$\therefore \quad y = AC$

Hence Proved.

(ii) $ABC + A\bar{B}C + AB\bar{C} = A(B + C)$

Let $y = ABC + A\bar{B}C + AB\bar{C}$

$= AC(B + \bar{B}) + AB\bar{C}$

$= AC + AB\bar{C}$ $\quad (\because B + \bar{B} = 1)$

$= A(C + B\bar{C})$

$= A(C + B)$ $\quad (\because A + \bar{A}B = A + B)$

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$$\therefore \quad y = A(B + C) \qquad (\because A + B = B + A)$$

Hence Proved.

Q. 2. (a) Simplify the function using K-Map

Σ (3, 6,7,10,11,13,14,15)

and give the logic circuit to realize this function.

Ans. K-Map

$$F(ABCD) = \Sigma (3, 6, 7, 10, 11, 13, 14, 15)$$

AB/CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	3	2
$\bar{A}B$	4	5	7	6
AB	12	13	15	14
$A\bar{B}$	8	9	11	10

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Quad 1: $m_3 + m_7 + m_{15} + m_{11} = CD$

Quad 2: $m_{10} + m_{11} + m_{14} + m_{15} = AC$

Quad 3: $m_6 + m_7 + m_{14} + m_{15} = BC$

Pair 1 : $m_{13} + m_{15} = ABD$

$(CD) + (AC) + (BC) + (ABD)$

(b) What is an encoder? Draw a circuit for a decimal to binary encoder and explain its functioning. 7½

Ans. An encoder is a logic circuit which converts digits and/or some special symbols to a binary coded format. It has n inputs and m outputs.

Q. 3. (a) Draw a circuit for a 4 bit adder subtractor and explain its working. 7½

Ans. The addition and subtraction operation can be combined into one common circuit by inncluding an exclusive—OR gate with each full-adder. A 4-bit adder-subtractor circuit is shown is fig. The mode input m controls the operation.

When M = 0, the circuit is an adder and when M = 1, the circuit becomes a subtractor.

Each exclusive–OR gate receives input M and one of the input of B. When M = 0, we have B ⊕ 0 = B. The full adders receives. The value of B, the input carry os 0 and circuit performs A plus B.

When M = 1, we have $B \oplus 1 = B'$ and $C_0 = 1$

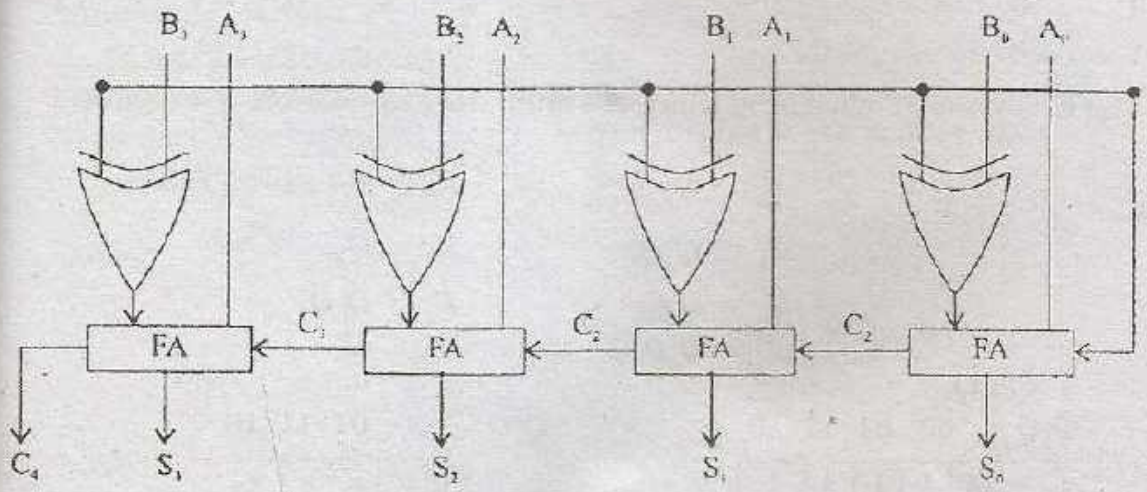

Fig. 4-bit adder-subtractor

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The B inputs are all complemented and 1 is added through the input carry. The circuit performs the operation A-plus the 2's complement of B, this give A–B.

If we use two given number

A = 1111 and B = 100, then circuit work both ways like adder and subtracter and finally we get the result.

(b) What are shift registers? What type of shift register is the fastest? Realize a 4-bit SIPO shift register using block diagram of SR flip flop. 7½

Ans. See Q. 2, Page 201

Q. 4. (a) Explain working of a decade counter with the help of a circuit diagram. 7½

Ans. DecadeCounter. A decade up counter can be designed using J-K flip-flops. There are ten states in a decade counter. Four flip-flops are required for the purpose. The remaining six states are n used states.

The following table gives the count sequence and the flip-flop inputs.

Counter state				*Flip flop inputs*							
Q_3	Q_2	Q_1	Q_0	J_0	K_0	J_1	K_1	J_2	K_2	J_3	K_3
0	0	0	0	1	×	0	×	0	×	0	×
0	0	0	1	×	1	1	×	0	×	0	×
0	0	1	0	1	×	×	0	0	×	0	×
0	0	1	1	×	1	×	1	1	×	0	×
0	1	0	0	1	×	0	×	×	0	0	×
0	1	0	1	×	1	1	×	×	0	0	×
0	1	1	0	1	×	×	0	×	0	0	×
0	1	1	1	×	1	×	1	×	1	1	×

1	0	0	0	1	×	0	×	0	×	×	0
1	0	0	1	×	1	0	×	0	×	×	1
0	0	0	0							

The K-maps are shown from which the minimized expressions are obtained as

$J_0 = 1,$ $K_0 = 1$

$J_1 = Q_0\bar{Q}_3$ $K_1 = Q_0$

$J_2 = Q_0Q_1$ $K_2 = Q_0Q_1$

$J_3 = Q_0Q_1Q_2$ $K_3 = Q_0$

J_0

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	1	1	×	1
01	×	×	×	1×
11	×	×	×	×
10	1	1	×	×

K_0

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	×	×	×	×
01	1	1	×	1
11	1	1	×	×
10	×	×	×	×

J_1

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	0	0	×	0
01	1	1	×	0
11	×	×	×	×
10	×	×	×	×

K_1

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	×	×	×	×
01	×	×	×	×
11	1	1	×	×
10	0	0	×	×

J_2

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	0	×	×	0
01	0	×	×	0
11	1	×	×	×
10	0	×	×	×

K_2

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	×	0	×	×
01	×	0	×	×
11	×	1	×	×
10	×	0	×	×

J_3

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	0	0	×	×
01	0	0	×	×
11	0	1	×	×
10	0	0	×	×

K_3

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	×	×	×	0
01	×	×	×	1
11	×	×	×	×
10	×	×	×	×

The circuit can be drawn using the above expressions.

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(b) Draw the block diagram of a cathode ray oscilloscope and explain how it is used to calculate amplitude and frequency of a sinusoidal wave. 7½

Ans. The cathode ray oscilloscope (CRO) provides a visual presentation of any wave-form applied to the input terminals. An electron beam is deflected as it sweeps across the tube face, leaving a display of the applied signal.

Block Diagram

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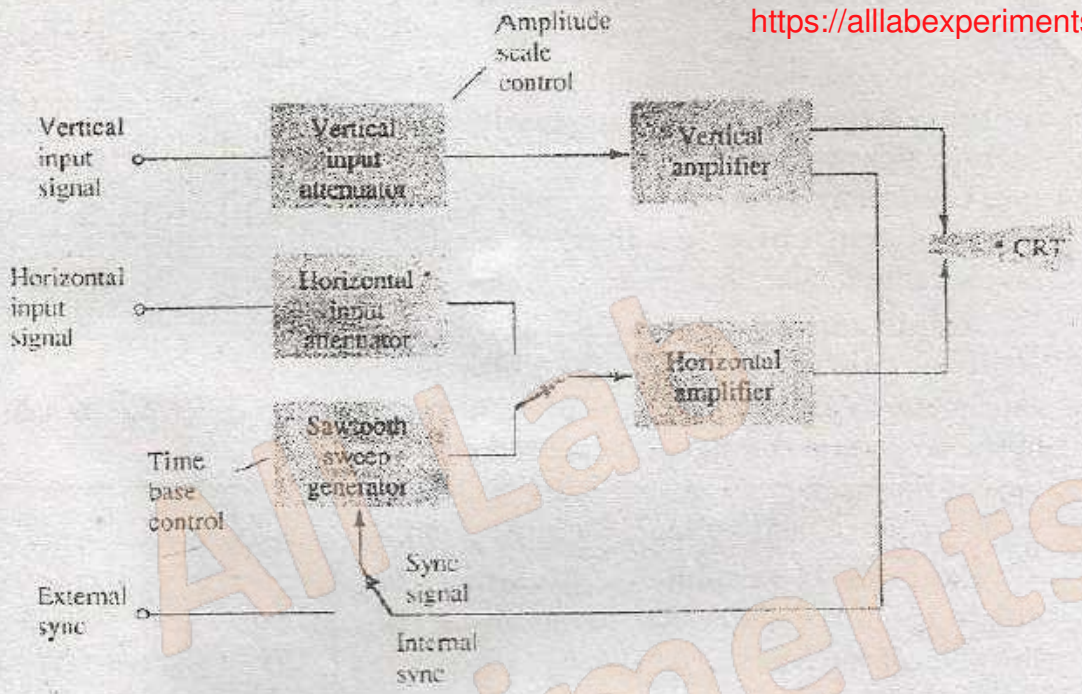

The basic parts of a CRO are shown in Fig. above . We will first consider the CRO's operation for this simplified block diagram. To obtained a noticeable beam deflection from a centimeter to a few centimeters, the usual voltage applied to the deflection plates must be on the order of tens to hundreds of volts. Since the singals measured using a CRO are typically only a few volts, or even a few millivolts, amplifier circuits are needed to increase the input signal to the voltage levels required to operate the tube. There are amplifier sections for both the vertical and the horizontal deflection of the beam. To adjust the level of a signal, each input goes through an attenuator circuit which can adjust the amplitude of the display.

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Cathode ray Oscilloscope Operation.

For operation as an oscilloscope the electron beam is deflected horizontally by a sweep voltage, and vertically by the voltage to be measured. While the electron beam is moved across the face of the CRT by the horizontal sweep signal, the input signal deflects the beam vertically, resulting in a display of the input signal waveform. One sweep of the beam across the face of the tube, followed by a "blank" period during which the beam is turned off while being returned to the starting point across the tube face, constitutes one sweep of the beam

A steady display is obtained when the beam repeatedly sweeps across the tube with exactly the same image each sweep. This requires a synchronization, starting the sweep at the same point in a repetitive waveform cycle. If the signal is properly synchronized, the display will be stationary, In the absence of sync the picture will appear to drift or move horizontally across the screen.

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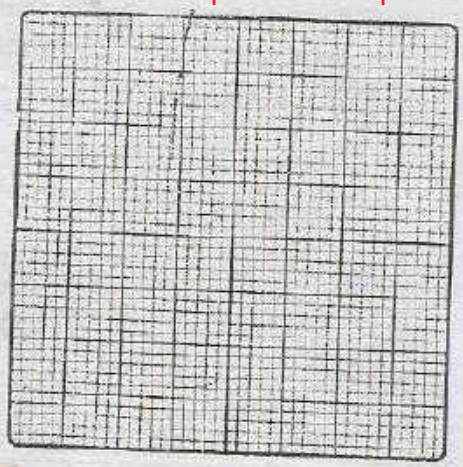
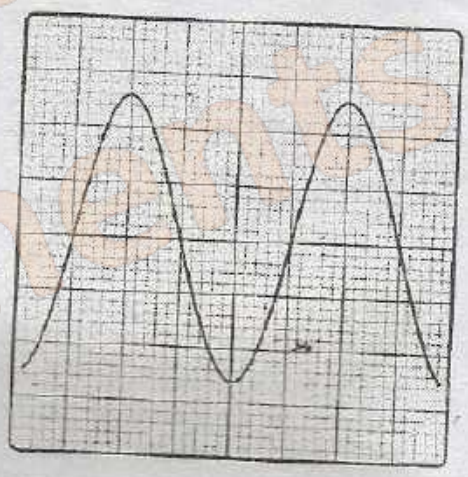


Measurment Using Calibrated CRO Scales. The oscilloscope tube face has a calibrated scale to use in making amplitude or time measurements. Figure shows a typical calibrated scale. The boxes are divided into centimeters (cm), 4 cm on each side of center. Each centimeter (box) is further divided into 0.2-cm intervals.

Amplitude Measurments. The vertical scale is calibrated in either volts per centimeter (V/cm), or millivolts per centimeter (mV/cm). Using the scale setting of the scope and the signal measured off the face of the scope, one can measure typically peak to peak or peak voltages for an ac signal.



Example 1: Calculate the peak-to-peak amplitude of the sinusoidal signal in Fig. if the scope scale is set to 5 mV/cm.

Ans. The peak to peak amplitude is

$$2 \times 2.6 \text{ cm} \times 5 \text{mV/cm} = 26 \text{ mV}$$

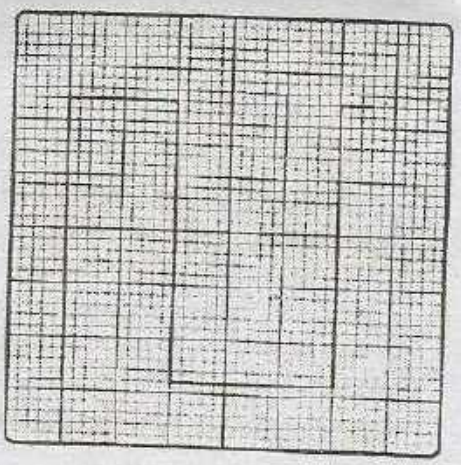
Example 2 : Calculate the amplitude of the pulse signal in Fig. (scope setting 100 mV/cm).

Ans. The peak-to-peak amplitude is

$$(2.8 \text{ cm} + 2.4 \text{ cm}) \times 100 \text{ mV/cm} = 520 \text{ mV} = 0.52 \text{ V}$$

Time Measurements

Period. The horizontal scale of the scope can be used to measure time, in seconds (s), milliseconds (ms), microseconds (μs), or nanoseconds (ns). The interval of a pulse from start to end is the period of the pulse. When the signal is repetitive, the period is one cycle of the waveform.



Example 3: Calculate the period of the waveform shown in Fig. 20 μs/cm.

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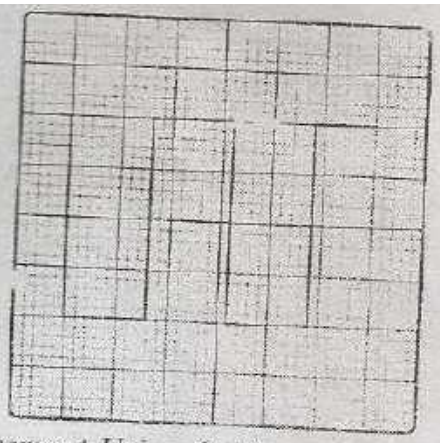


Measurement Using Calibrated CRO Scales

Ans. For the waveform of above Fig.

Period = $T = 3.2 \text{ cm} \times 20 \text{ (}\mu\text{s/cm} = 64\mu\text{s}$

Frequency. The measurement of a repetitive waveform's period can be used to calculate the signal's frequency. Since frequency is the reciprocal of the period.

$$f = \frac{1}{T}$$

Example 4 : Determine the frequency of the waveform shown in Fig. of last Ex. (scope setting at 5 μ/cm)

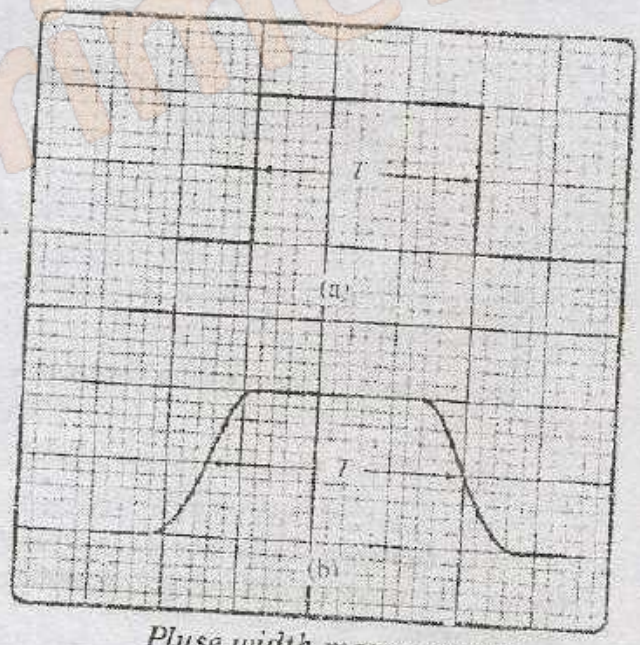
Solution From the waveform

Period = $T + 3.2 \text{ cm} \times 5\mu\text{s/cm} = 16 \mu\text{s}$

$$f = \frac{1}{T} = \frac{1}{16 \mu s} = 62.5 \text{ kHz}$$

Pulse width. The time interval that a waveform is high (or low) is the pulse width of the signal. When the waveform edges go up and down instantly the width is measured from start (leading edge) to end (trailing edge) (see Fig (a)) For a waveform with edges that rise or fall over some time the pulse width is measured between the 50% points as shown in Fig.(b).

Example 5 : Determine the pulse width of the waveform in Fig.



Pluse width measurement

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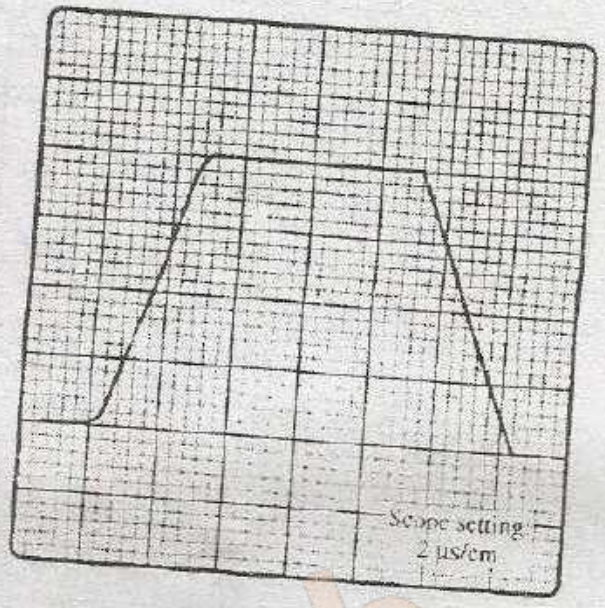
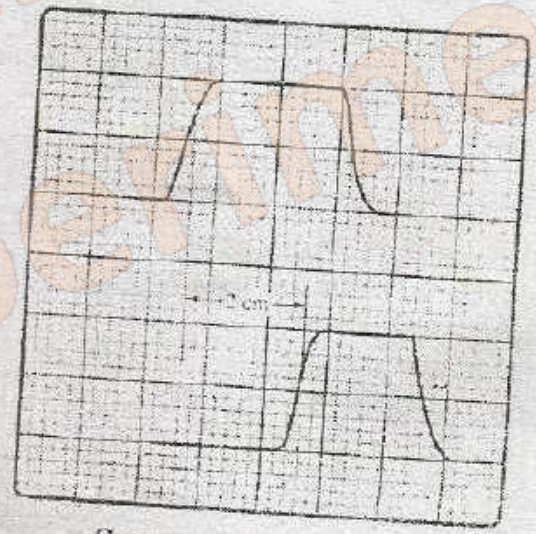


Ans. For a reading of 4.6 cm at the midpoint of the waveform the pulse width is

$$T_{pw} = 4.6 \text{ cm} \times 2 \text{ μs/cm} = 9.2 \text{ μs}$$

Pulse Delay. The time interval between pulses is called the pulse delay. For waveforms, as shown in Fig. the pulse delay is measured between the midpoint (50% point) at the start of each pulse.



Scope setting 50 μ/cm

Example 6 : Determine the pulse delay for the waveforms of above Fig.

Ans. From the waveforms in Fig.

$$\text{pulse delay} = T_{pp} = 2 \text{ cm} \times 50 \text{ μs/cm} = 100 \text{ μs}$$

Q. 5. (a) Draw the circuit of an Astable Multivibrator using IC 555 imer IC and explain its operation. Derive the expression for its requency.

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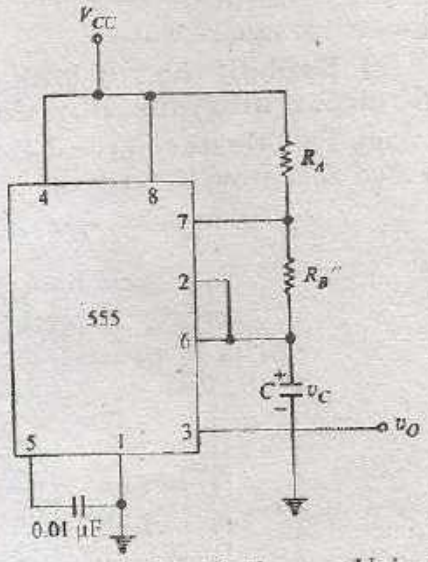
Ans. Astable Multivibrator. An astable or free running multivibrator is a square wave generator.

An astable multivibrator using 555 timer is shown. Let us assume that the output is in HIGH state and the capacitor C is charging through resistors R_A and R_B [time constant $\tau_1 = (R_A + R_B)$ C]. When the voltage across $C(v_c)$ reaches 2/3 V_{cc}, the output goes LOW and C starts discharging through R_B with a time constant $\tau_2 = R_B$. C. When v_c drops below $V_{cc}/3$, the timer is triggered and the output again goes HIGH. The capacitor C now again starts charging towards V_{cc} with the time constant τ_1. The various waveforms are shown below. The charging and discharging time intervals are given by



An Astable Multivibrator Using 555

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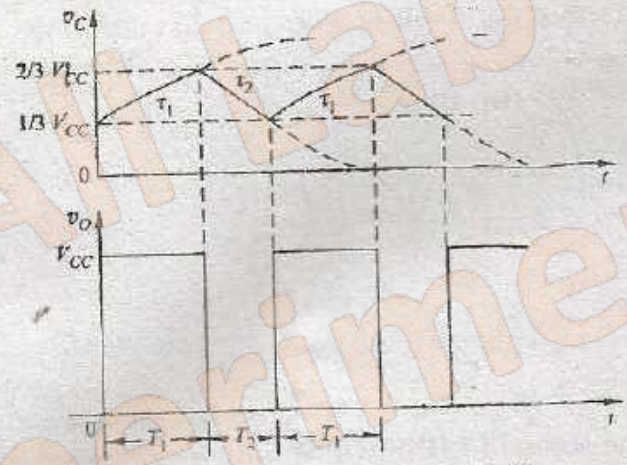

Waveforms of 555 Astable Multivibrator

The charging and discharging time intervals are given by

$$T_1 = 0.7\,C\,(R_A + R_B) \quad \text{...(i)}$$

and

$$T_2 = 0.7CR_B \quad \text{...(ii)}$$

Therefore,

$$f = \frac{1}{T} = \frac{1}{T_1 + T_2} = \frac{1.4}{C(R_A + 2R_B)} \quad \text{...(iii)}$$

and the duty cycle

$$D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\% \quad \text{...(iv)}$$

From Eq. (iv) we note that the duty cycle is always different from 50%. It can be made 50% (symmetrical square wave) by connecting a diode across R_B, which will clamp the voltage across R_B when the capacitor is charging and therefore if R_A and R_B are equal, t_1 and t_2 will be same. It is also possible to generate a symmetrical square wave by using the output of 555 as clock input of

a T-type FLIP-FLOP with $T = 1$. The output of the FLIP-FLOP will be a symmetrical square wave.

(b) Explain the working of a MASTER-SLAVE JK flip flop using logic circuit diagram. How does it overcome racing problem. 7½

Ans. The Master Slave J-K flip-flop. It is a cascade of two S-R flip-flops. The feed back from the outputs of the second act as inputs of the first.

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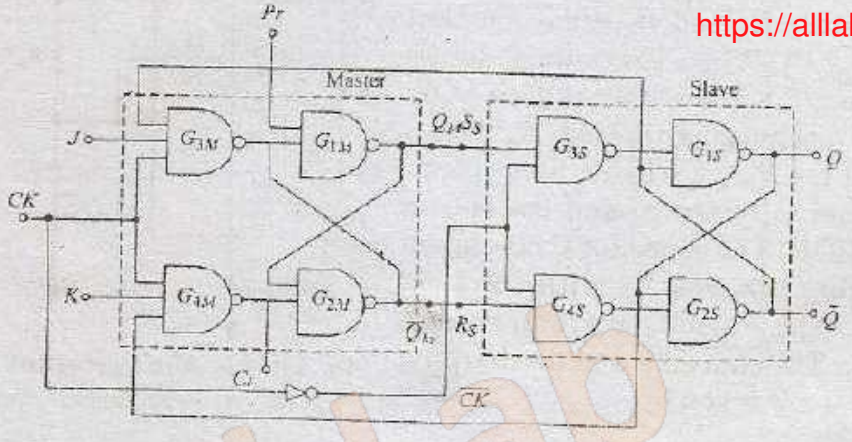

When CK= 1, the first flip-flop is enabled and the outputs Q_m and $\bar{Q}_m$ respond to inputs J and K as below

Truth Table of J-K flip flop

Inputs		*Outputs*
J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

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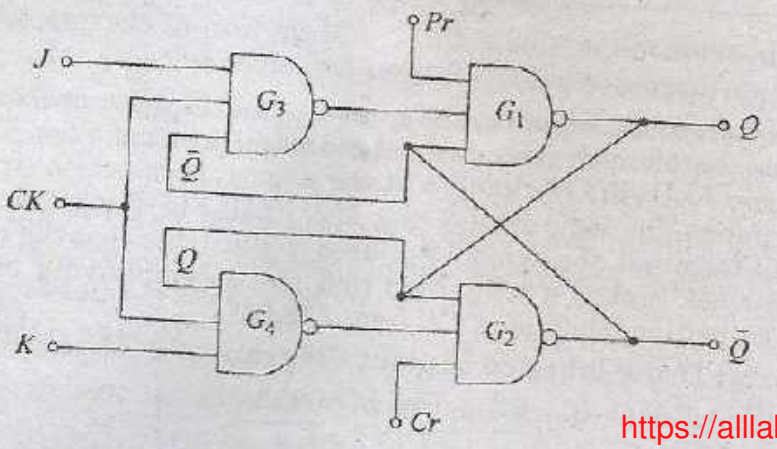
At this time, the second FLIP-FLOP is inhibited because its clock is LOW $(\overline{CK} = 0)$. When CK goes LOW $(\overline{CK} = 1)$, the first FLIP-FLOP is inhibited and the second FLIP-FLOP is enabled, because now its clock is HIGH $(\overline{CK} = 1)$.

Therefore, the outputs Q and $\bar{Q}$ follow the outputs Q_M and $\bar{Q}_M$, respectively (second and third rows of Table). Since the second FLIP-FLOP simply follows the first one, it is referred to as the *slave* and the first one as the *master*. Hence, this configuration is referred to as master—slave (*M-S*) FLIP-FLOP.

The Race Around Condition. The difficulty of both inputs 1 ($S = R = 1$) is not allowed in an S-R flip-flop. This is elminated in a J-K flip-flop by using the feedback connetion from outputs to the inputs of the gates G_3 and G_4.



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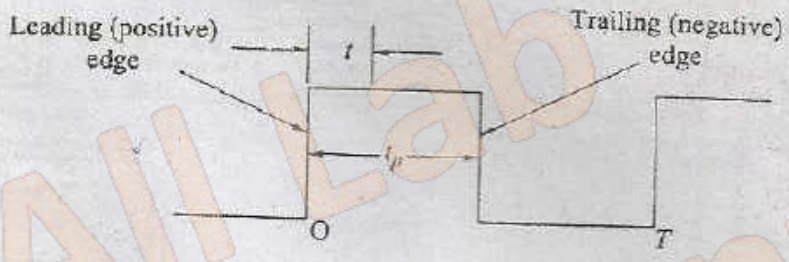
AJ-K Flip flop Using NAND gates

We assume that the inputs do not change during the clock pulse *(CK=1)*. This is not correct due to feedback connections.

Consider that the inputs are $J = K = 1$ and $Q = 0$, and A pulse as shown below is applied at the



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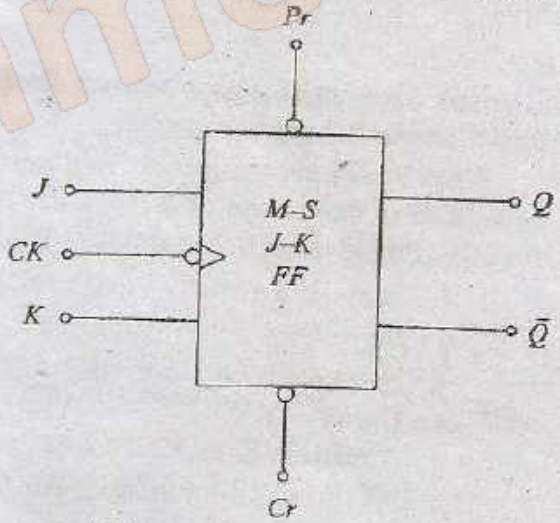
A clock Pulse

Clock Input. After a time interval Δt equal to the propagation delay through two NAND gates in series, the output will change to $Q = 1$ (see fourth row of Table). Now we have $J = K = 1$ and $Q = 1$ and after another time interval of Δt the output will change back to $Q = 0$. Hence, we conclude that for the duration t_p of the clock pulse, the output will oscillate back and forth between 0 and 1. At the end of the clock pulse, the value of Q is uncertain. This situation is referred to as the race-around condition.

The race-around condition can be avoided if $t_p < \Delta t < T$. However, it may be difficult to satisfy this inequality because of very small propagation delays in ICs. A more practical



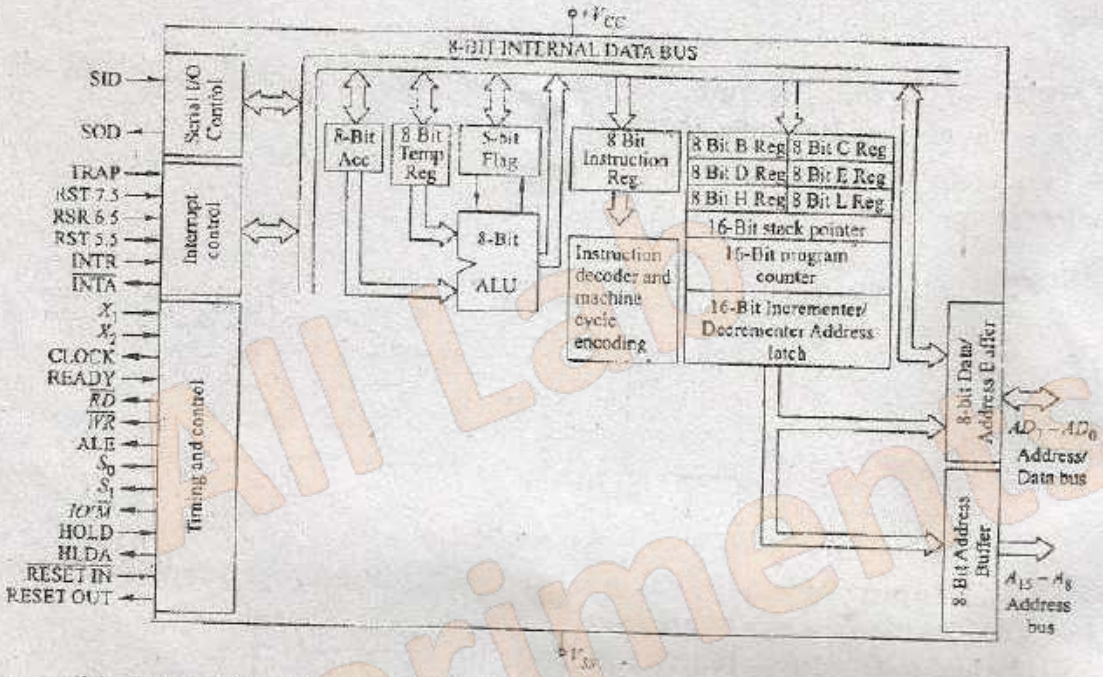
A Master-Slave J-K FLIP - FLOP
Logic Symbol

method for overcoming this difficulty is the use of the master-slave (*M–S*) configuration discussed below.

In this circuit, the inputs to the gates G_{3M} and G_{4M} do not change during the clock pulse, therefore the race-around condition does not exist. The state of the master-slave FLIP-FLOP changes at the negative transition (trailing edge) of the clock pulse. The logic symbol of a *M-S* FLIP-FLOP is given in Fig.. At the clock input terminal, the symbol > is used to illustrate that the output changes when the clock makes a transition and the accompanying bubble signifies negative transition (change in *CK* from 1 to 0).

Q. 6. (a) Draw labelled pin out diagram of 8085 microprocessor. 5

Ans. Functional Block diagram of 8085A Microprocessor



(b) Describe the various flags used in 8085 microprocessor and show their bit positions.

Ans. Flags are single bit registers used to store certain conditions which arise due to execution of certain arithmatic and logical operations. There are five flip-flops which are referred to as flags.

1. Zero (Z)
2. Sign (S)
3. Parity (P)
4. Carry (CY)
5. Auxiliary carry (AC)

Zero. If the result of an operation is zero, the zero flag is set, otherwise it is reset.

Sign. If the result of an operation produces 1 as MSB in the accumulator, the sign flag is set, otherwise it is reset.

Parity. If the result of an operation makes the parity of the bits in the accumulator even, the parity flag is set, otherwise it is reset.

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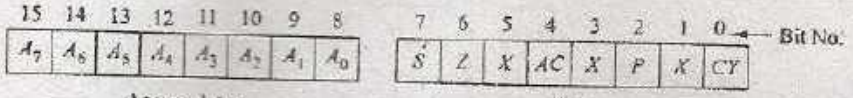
Carry. If a carry is generated from MSB as a result of certain operation, the carry flag is set (1), otherwise it is reset (0)

Auxiliary Carry. If an operation produces carry out from the lower order four bits, the auxiliary carry flag is set otherwise it is reset. It is used for BCD arithmetic.

Flag Setting. A flag is set by forcing the bit to 1 and reset by forcing the bit to 0. These flags can be accessed by some instructions alongwith the accumulator, as a single process status word (PSW).

Organisation of PSW



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There are two instructions STC (Set Carry) and CMC (Complement Carry) which directly address the carry flag.

The flags are examined in conditional instructions to deterine if the specified condition is true or false. The names and binary codes of the conditions are given below.

Condition name	Flag status	Binary code
NZ — Not zero	$Z = 0$	000
Z — Zero	$Z = 1$	001
NC — No carry	$CY = 0$	010
C — Carry	$CY = 1$	011
PO — Parity odd	$P = 0$	100
PE — Parity even	$P = 1$	101
P — Plus	$S = 0$	110
M — Minus	$S = 1$	111

(c) Write an assembly language program to multiply two eight bit number 04 H and 05H. Numbers are stored in memory location 2000H and 2001H. Store the result in 2002H. 5

Ans. Consult your textbook.

Q. 7. (a) How Demultiplexing of address bus and data bus is done in 8085 microprocessor. Explain with the help of timing diagram. 10

Ans. Demultiplexer. A DMUX is a combination logic circuit that recieves information on a single line and transmits this information one of the many output lines.

Demultiplexer performs the reverse operation of MUX. The functional diagram of a DMUX is shown in Fig. (a). The circuit has one input signal m control select inputs and n output signals. The select input code determines to which output the DATA input will be transmitted. As the serial data is changed to parallel data, the multiplexer is also called a distributor or decoder.

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Truth Table for 1 to 4 DMUX

Selesct INPUTs		OUTPUTS			
S_1	S_0	y_0	y_1	y_2	y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

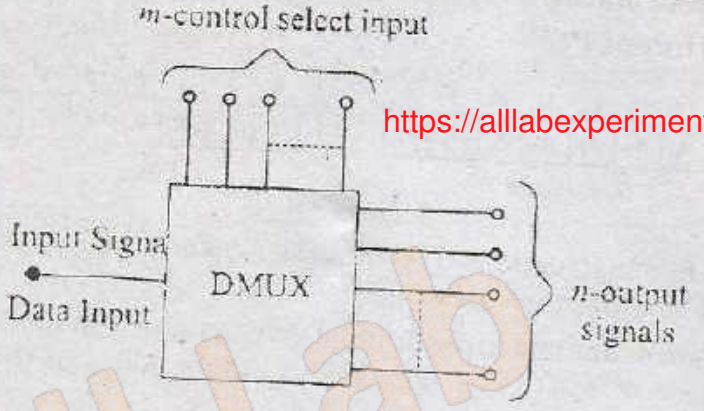

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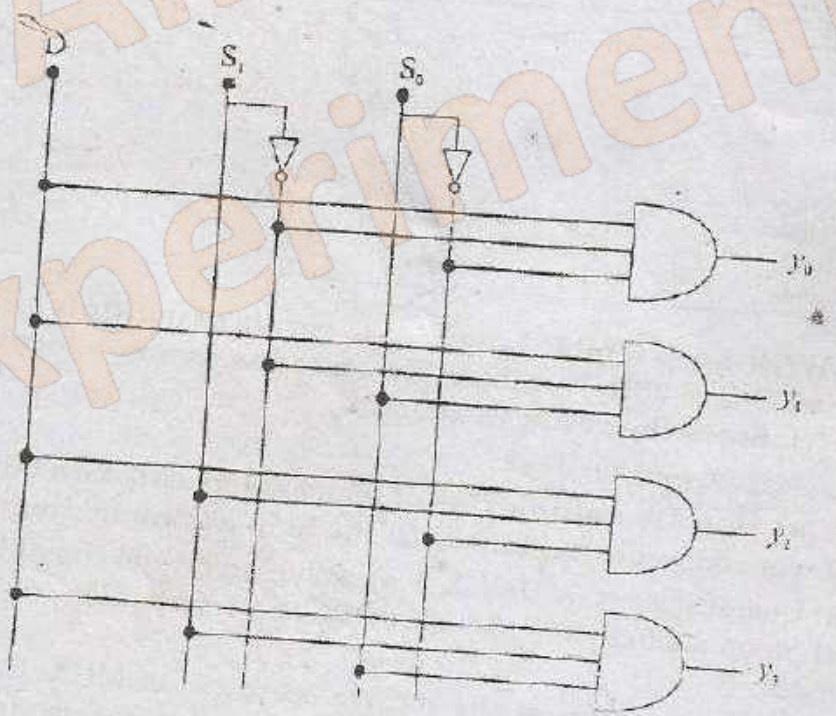
Fig. (a) Block diagram of DMUF

Logic circuit for 1 to 4 DMUX



(b) Write an assembly language program to add two sixteen bit numbers FDFF H and 0101 H.

Ans. Consult your textbook.