EXPERIMENT JUNCTION FIELD EFFECT TRANSISTOR (JFET)

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EXPERIMENT NO. 4

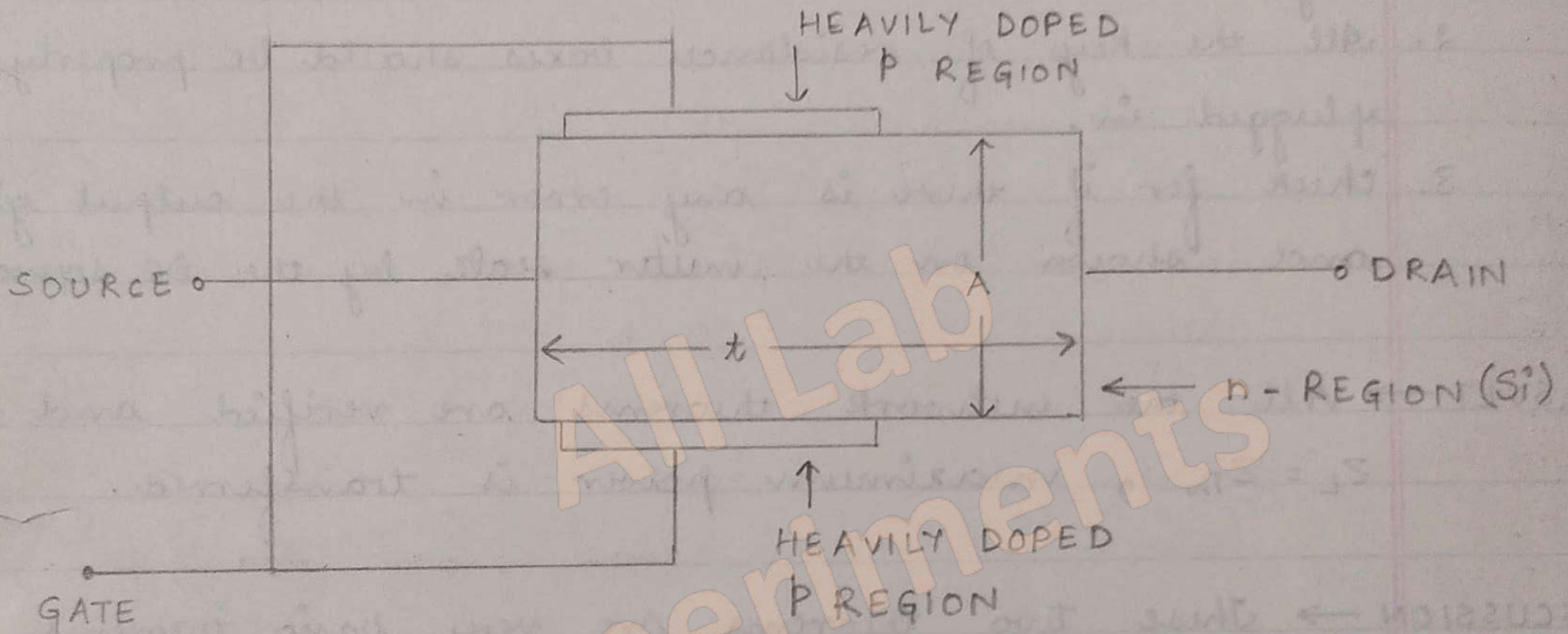
AIM → To study the output and transfer characteristics of a Junction Field Effect Transistor.

APPARATUS → FET Board (Model - B006), DC Voltmeters (0-30 V and 0-10 V), CRO, AF generator, DC microammeter (0-50 μA), DC milliammeter (0-10 mA).

THEORY → A JFET is a solid state device having V-I characteristics. It has three terminals called the SOURCE, DRAIN and the GATE. The gate to source bias voltage produces an electric field which controls the current flow from source to drain.

A FET consists of a n-type Si bar called channel (FIG 1). On both sides of this channel two heavily doped p-regions are created which are shorted together to form one terminal called the gate. The two ends of the channel are called the source and the drain. The p-regions form to two p-n junctions with the channel.

Suppose a -ve voltage is applied at the gate

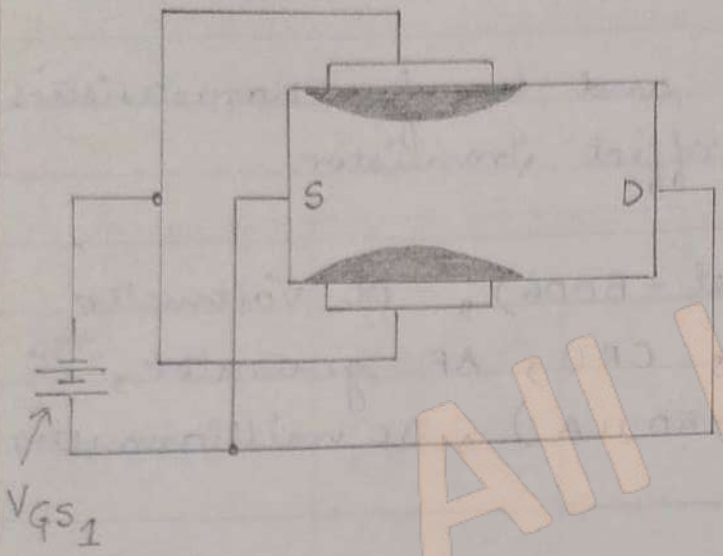


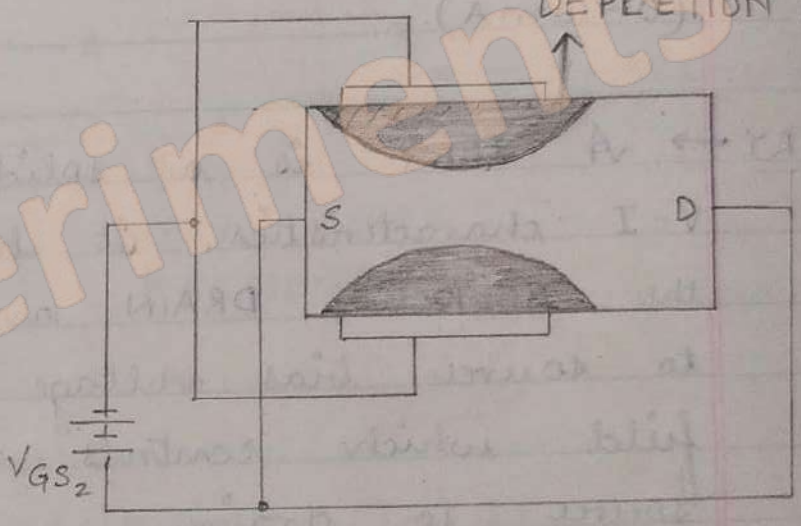
FIELD EFFECT TRANSISTOR (FIG. 1).

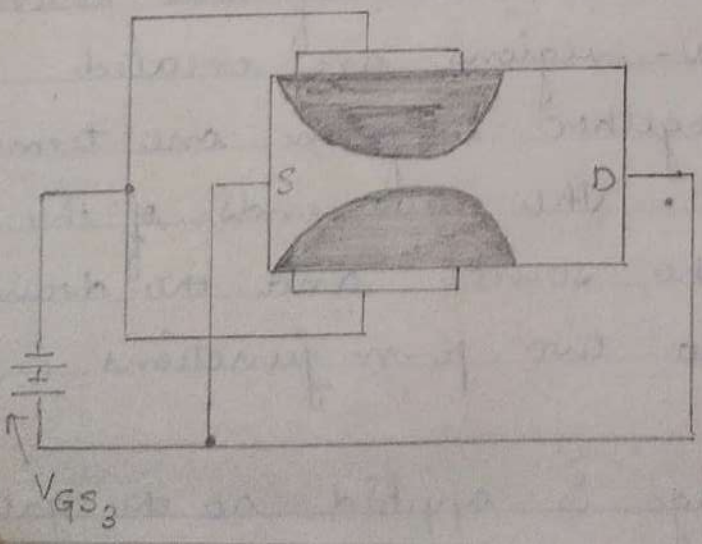
EFFECT OF V_{GS} ON EFFECTIVE AREA OF THE CHANNEL.

(FIG. 2)

$|V_{GS_3}| > |V_{GS_2}| > |V_{GS_1}|$







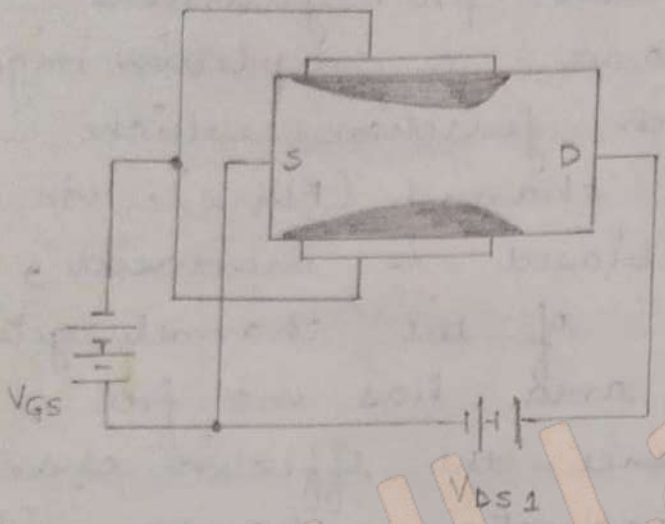
wrt the source, then two pn - junctions become reverse biased and a depletion region is developed around each junction which extends mostly into the channel (FIG. 2). As the magnitude of reverse biased is increased, more and more area of the channel gets depleted. The depleted area has no free charge carriers and hence the effective channel width available for conduction changes with the amount of reverse bias V_{GS}. Thus, the current flow through the channel can be controlled by the voltage applied at the gate.

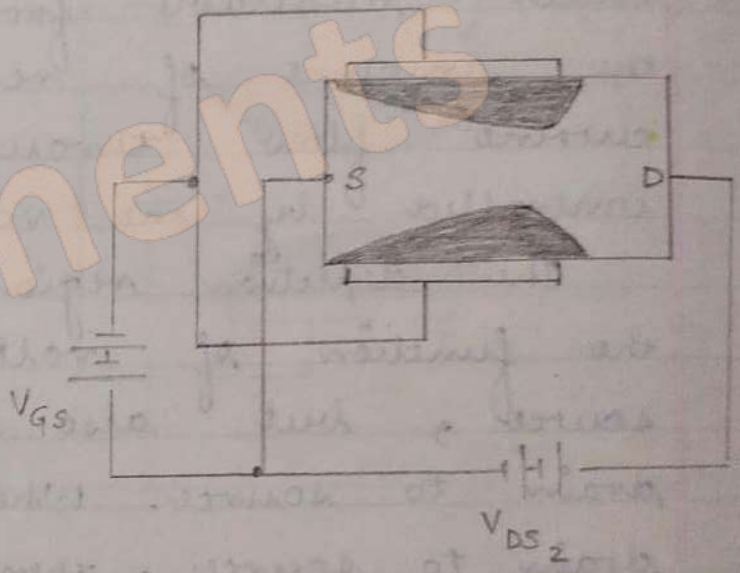
The depletion region widths are not only the function of voltage between gate and source, but also of the voltage drop from drain to source. When no current flows from drain to source, then no voltage drop exists between them and the depletion region widths are controlled only by the voltage V_{GS}. If a +ve drain to source voltage is applied across the channel, then the current flow in the channel will produce a voltage drop in it. The drain end will be more +ve than the source end and hence the reverse bias of the junctions will be more on the drain side

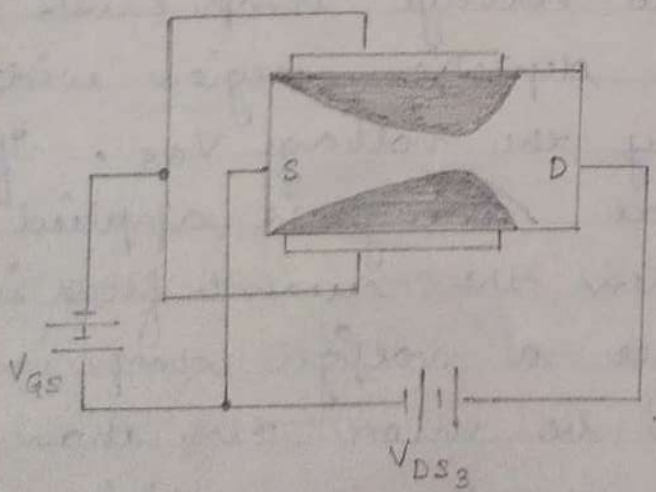
EFFECT OF V_{DS} ON EFFECTIVE AREA OF THE CHANNEL

(FIG. 3)

$V_{DS_3} > V_{DS_2} > V_{DS_1}$







than on the source side. This results in greater depletion region widths near the drain than those near the source (FIG 3).

Thus, the depletion region widths in the channel and hence the current through the channel depends on the voltage applied between the source and the voltage drop from drain to source. For small values of V_{DS}, the channel behaves like a voltage controlled resistor with V_{GS} behaving as the controlling voltage. As V_{DS} inc the reverse bias of the junctions inc towards the drain end and the effective channel area dec. The overall resistance of the channel increases. Now the changes in the drain current with V_{DS} become smaller and the rounding off the curves starting taking place. Ultimately, as V_{DS} is increased further, the effective channel width becomes zero at one point along the channel (FIG. 5). At this point the maximum depletion widths are equal to the half of the channel width. This situation is called PINCH - OFF. When Pinch - Off occurs the current flowing prior to Pinch - Off, becomes constant and there is not much change in current with V_{DS}, since most of the additional voltage applied, drops across the high resistance region of the channel.

If V_{GS} approaches some large negative value, the entire channel is depleted off free carriers and the drain current is approx. zero for all values of V_{DS}. The value of V_{GS} to reach this condition is called PINCH-OFF VOLTAGE, V_p. Near the drain end of the channel the effective reverse bias is $V_{GS} - V_{DS}$. Whenever $V_{GS} - V_{DS} = V_p$, the FET enters the Pinch-Off Region. With $V_{GS} = 0$, the FET enters Pinch-Off at $V_{DS} = V_p$. The drain current with $V_{GS} = 0$ and $V_{GS} = V_p$ is called short circuit drain current, I_{DSS}.

TRANSFER CHARACTERISTICS → This curve gives a relationship between drain current and gate-to-source voltage. The slope of this curve called Forward transconductance (g_m), is an important parameter in FET amplifier design.

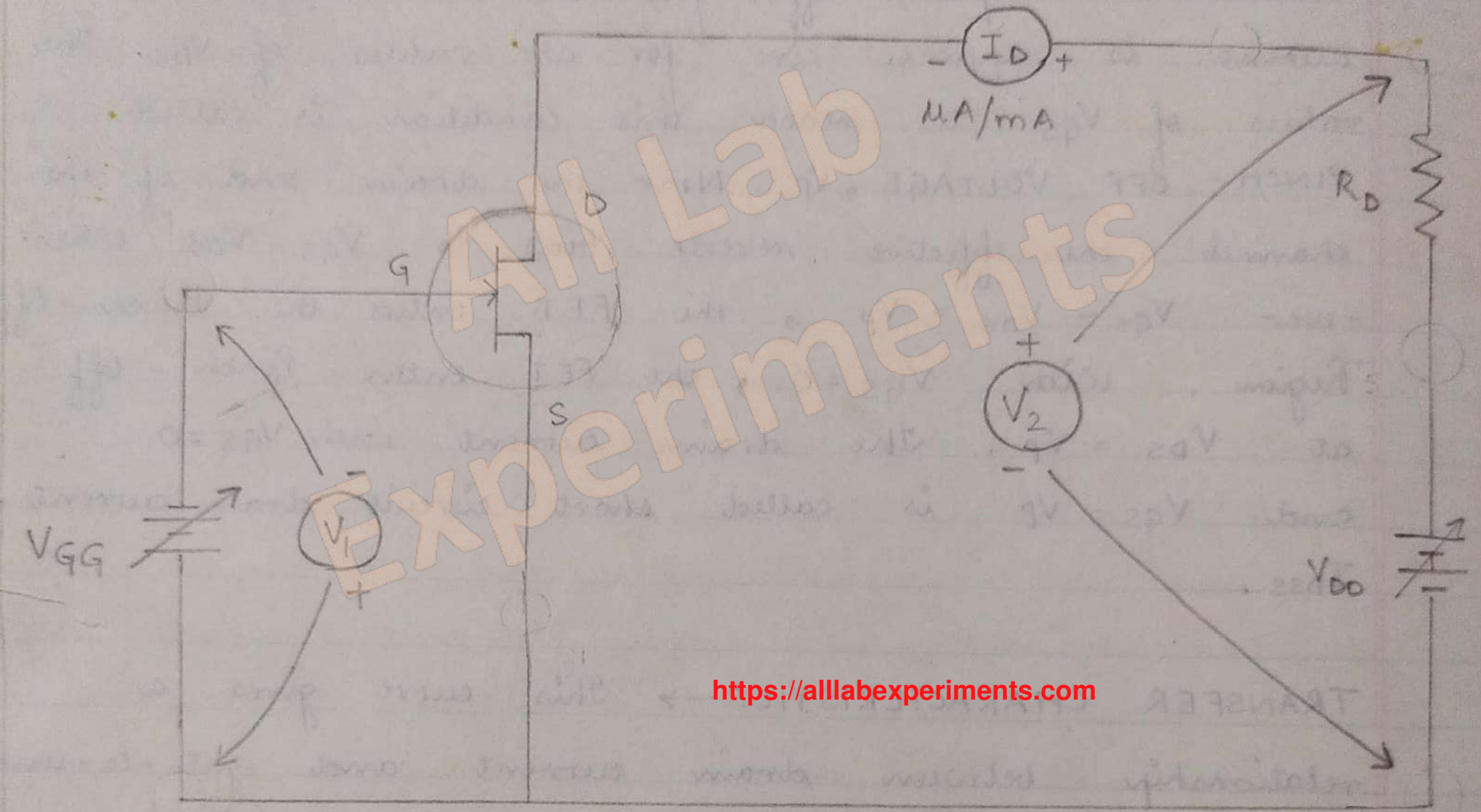
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{— 1.}$$

Slope of this curve is different at different points and so the transconductance is defined as,

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{— 2}$$

where g_{mo} = value of g_m for $V_{GS} = 0$

CIRCUIT DIAGRAM.



and is given as

$$g_m = -2\frac{I_{DSS}}{V_P} \quad \text{---- (3)}$$

g_{mo} is always positive.

PROCEDURE → I. MEASUREMENT OF PINCH-OFF VOLTAGE (V_P).

1. Arrange the set-up shown in the figure. Keep V_{DS} fixed at 8 V. For connecting the source to ground, short the terminals T_1 to T_2.
2. Increase V_{GG} and note that the current I_D decreases. Increase V_{GG} such that current I_D becomes zero.
3. Note the value of V_{GS} for the above condition and record it as V_P.

II. OUTPUT CHARACTERISTICS.

1. Arrange the setup as shown in figure.
2. Set $V_{GS} = V_P$ and keep it constant.
3. Vary V_{DD} in steps so as to change V_{DS} by about 0.1 V.
4. Set V_{GS} to a values about 0.25 less than V_P and repeat step 3. ~~Set~~ Repeat step 3 for different values of V_{GS} going upto $V_{GS} = 0$ V. For keeping $V_{GS} = 0$, disconnect the power supply V_{GG} and short the terminals T_1 and T_2.

5. Record the observations.

6. Choosing a suitable scale plot the observations on a linear graph paper. Keep I_D on Y-axis, V_{DS} on X-axis, V_{GS} as a parameter. This family of curves is the output characteristics of FET.

III. TRANSFER CHARACTERISTICS.

1. Arrange the set up shown in the figure.
2. Set V_{GS} to any value less than V_p.
3. Set V_{DD} so that V_{DS} is about 8V and some current I_D flows. Note that this value of V_{DS}, as it is to be kept constant throughout the measurements by adjusting V_{DD}.
4. Set $V_{GS} = 0$ by disconnecting the V_{GG} supply and shorting the terminals T_1 and T_2. Adjust V_{DD} to bring V_{DS} to the value fixed in step 3. Note the value of I_D.
5. Disconnect the short ckt at T_1 and T_2 and connect V_{GG} supply.
6. Vary V_{GS} in steps of 0.1 V and note the value of I_D at each step after adjusting V_{DD} to keep V_{DS} constant at previously adjusted value. Take obs. for V_{GS} upto V_p.
7. Record the observations in the table.

8. Choosing a suitable scale, keep I_D on Y-axis and V_{GS} on X-axis. V_{GS} is negative here. This curve is the transfer characteristics of FET.

9. Find the slope of this curve at $V_{GS} = 0$. It gives the value of g_{mo}.

OBSERVATION TABLE ⟶

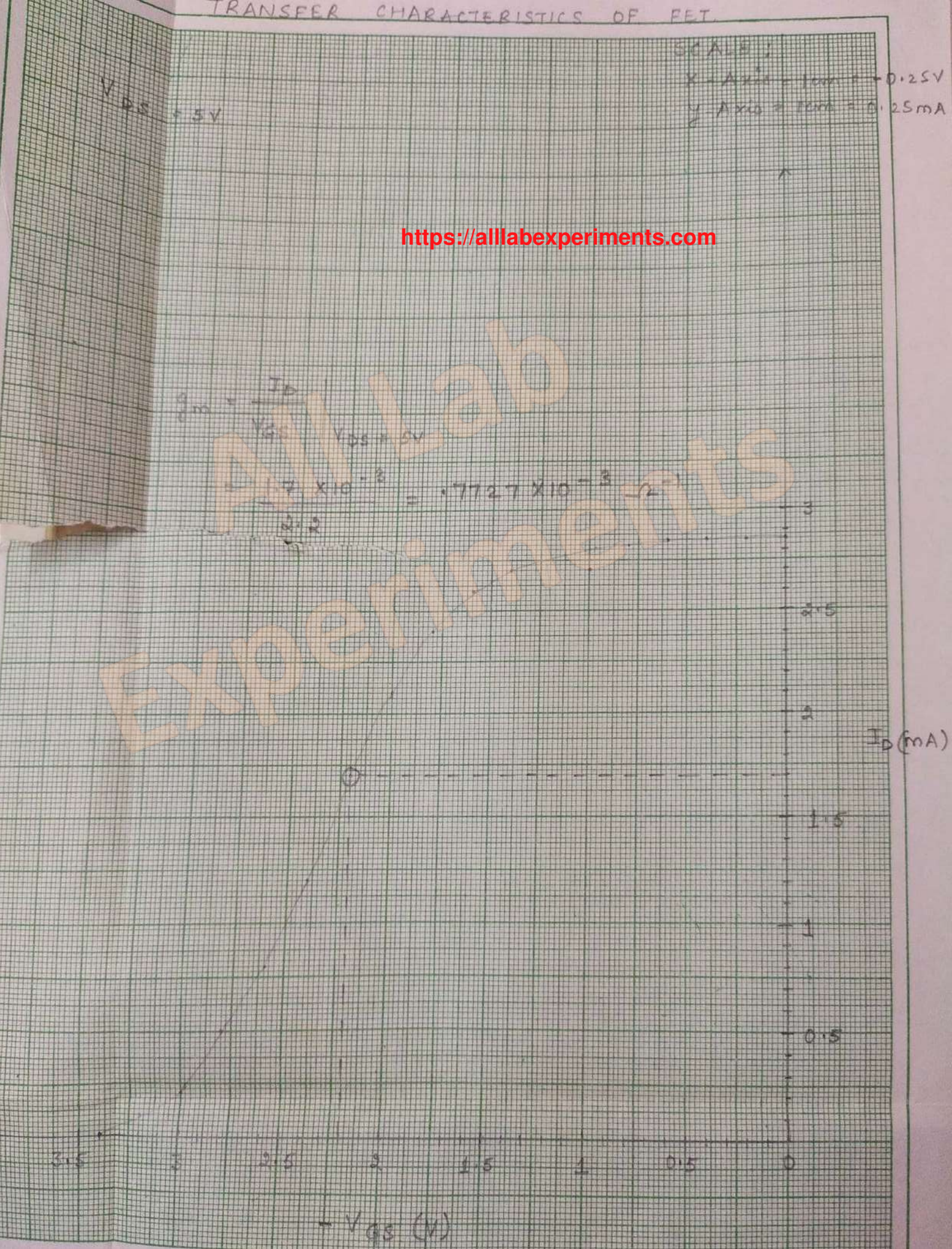
1. To measure the pinch-off voltage, V_P.

S. No.	V_{DS} = 8V		V_{DS} = 5V	
	$V_{GS} = V_{GG}$ (V)	I_D (mA)	$V_{GS} = V_{GG}$ (V)	I_D (mA)
1.	0	4.50	0	2.9
2.	0.2	4.45	0.2	2.85
3.	0.4	4.40	0.6	2.85
4.	0.6	4.40	0.8	2.8
5.	0.8	4.3	1.0	2.78
6.	1.0	4.2	1.2	2.75
7.	1.2	4.1	1.4	2.70
8.	1.4	3.85	1.6	2.6
9.	1.6	3.3	1.8	2.4
10.	1.8	2.8	2.0	2.0
11.	2.0	2.2	2.2	1.6
12.	2.2	1.7	2.4	1.1
13.	2.4	1.2	2.6	0.7
14.	2.6	0.7	2.8	0.4
15.	3.0	0.3	3.0	0.3
16.	3.2	0.1	3.2	0.2
17.	3.4.	0.00	3.4	0.1
			3.6	0

2. Output Characteristics.

V_{GS} = 2.5		V_{GS} = 2V		V_{GS} = 1.5V		V_{GS} = 1.0V		V_{GS} = .5V		V_{GS} = 0V	
V_{DS}(V)	I (mA)	V_{DS}	I	V_{DS}	I	V_{DS}	I	V_{DS}	I	V_{DS}	I
0	0	0	0	0	0	0	0	0	0	0	0
0.5	0.3	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0	0.5	0
1.0	0.45	0.2	0.1	0.4	0.2	0.4	0.2	0.4	0	1.	0.5
1.5	0.6	0.3	0.12	0.6	0.4	0.6	0.4	0.8	0	1.5	1
2.0	0.7	0.4	0.2	1	0.6	1.0	0.6	1.0	0.5	2.5	1.5
2.5	0.8	0.5	0.25	1.5	0.9	1.5	0.9	1.5	0.5	4.0	2
3.0	0.8	1.0	0.5	2.0	1.2	2.0	1.2	2.5	1	5.0	2.5
4	0.9	1.5	0.8	2.5	1.4	2.5	1.5	3.0	1.5	6.0	3.0
5	0.9	2.0	1.0	3.5	1.8	3.5	1.9	4.0	2	7.0	4
6	0.9	3.0	1.5	4.0	2.1	4.0	2.2	5.0	2.5	8.0	4.5
7	1	3.5	1.6	4.5	2.4	4.5	2.4	6.0	3.0	9.0	5
8.	1	4.0	1.7	5.0	2.5	5.0	2.8	7.0	3.5	11.0	6
⋮	⋮	5.0	2.0	6.0	3.0	6.0	3.0	8.0	4	13.0	7.5
20	1	6.0	2.1	7.0	3.4	7.0	3.8	9.0	5	14.0	8.0
		7.0	2.1	8.0	3.6	8.0	4.2	10.0	5.5	15.0	8.5
		8.0	2.2	9.0	3.7	9.0	4.5	11.0	6.0	16.0	9.0
		9.0	2.2	10.0	3.8	10.0	4.5	12.0	6.5	17.0	9.5
		10.0	2.3	11.0	3.9	11.0	4.5	13.0	7.0	18.0	10.0
		⋮	⋮	⋮	⋮	⋮	⋮	14.0	7.5	19.0	10.0
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	21.0	10.5
		20.	2.3	20	3.9	20	4.5	25.0	7.5	⋮	⋮
										30.0	10.5

TRANSFER CHARACTERISTICS OF FET



3. Transfer characteristics. $V_{DS} = 5V$

$V_{GG} = V_{GS}$ (V)	I_D (mA)	$V_{GG} = V_{GS}$ (V)	I_D (mA)
0	2.85	1.8	2.4
0.2	2.85	2.0	2.1
0.4	2.85	2.2	1.7
0.6	2.85	2.4	1.2
0.8	2.82	2.6	0.8
1.0	2.80	2.8	0.5
1.2	2.7	3.0	0.2
1.4	2.7	3.2	0.1
1.6	2.6	$3.4 \approx 3.5$	0.0

RESULT → From the transfer characteristics the Pinch Off Voltage is 3.4 V. The transconductance $g_m = .7727 \times 10^{-3} \Omega^{-1}$ and $r_d = 2.67 \times 10^3 \Omega$.

The Amplification factor $\mu = g_m r_d$

$= .7727 \times 10^{-3} \times 2.67 \times 10^3$

$= 2.06$

PRECAUTIONS → 1. The circuit should be wired properly.
2. The connections should be tight.
3. Proper scales for graph should be chosen.

DISCUSSION → The graph made by experiment are a bit different from the ideal characteristics because of the error in the apparatus. The transfer characteristics come out to be a smooth curve which is not as smooth as they should be.