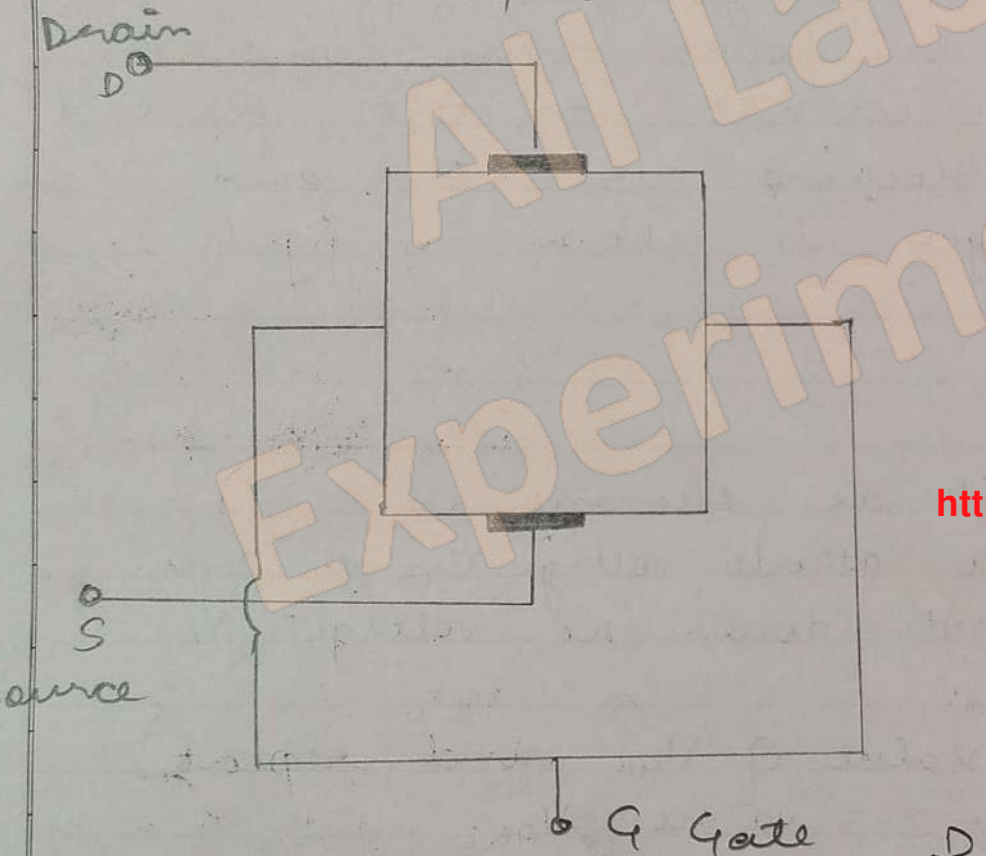
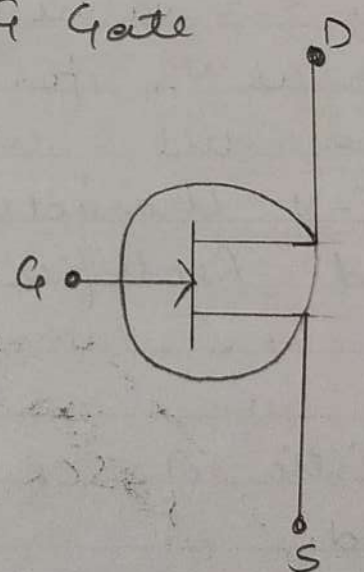
EXPERIMENT- 7

AIM:- To study the I-V characteristics of the Common Source (CS) configuration of FET.

Apparatus:- Variable d.c. regulated power supply, milliammeter (0-20 mA), voltmeters (0-20 V) and (0-2 V), resistors and FET.





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Theory :- The Field Effect Transistor (abbreviated as FET) is a three terminal unipolar semiconductor device in which current is controlled by an electric field. The Basic structure of JFET is shown in fig. on the opp. page. There are ~~two~~ three terminals.

1. Source
2. Drain
3. Gate

Standard Notations worthnotings FET are as follows:

1. **SOURCE :-** The terminal through which the majority carriers enter the channel, is called the source terminal S and the Conventional current entering the channel ~~is~~ at S is denoted by I_S.
2. **DRAIN :-** The terminal through which the majority carriers leave the

channel is called the drain terminal D and the conventional current leaving the channel at D is designated as I_D.

③ Gate :- There are two internally connected heavily doped impurity regions formed by alloying, by diffusion or by any other method available to create two p-n junctions. These impurity regions are called the gate G. A voltage V_{GS} is applied between the gate and source in the direction to reverse-bias the p-n junction.

④ Channel :- The region between the Source and the drain, sandwiched between the two gates is called the channel and the majority carriers move from the source to drain through this channel.

CHARACTERISTICS of FET :-

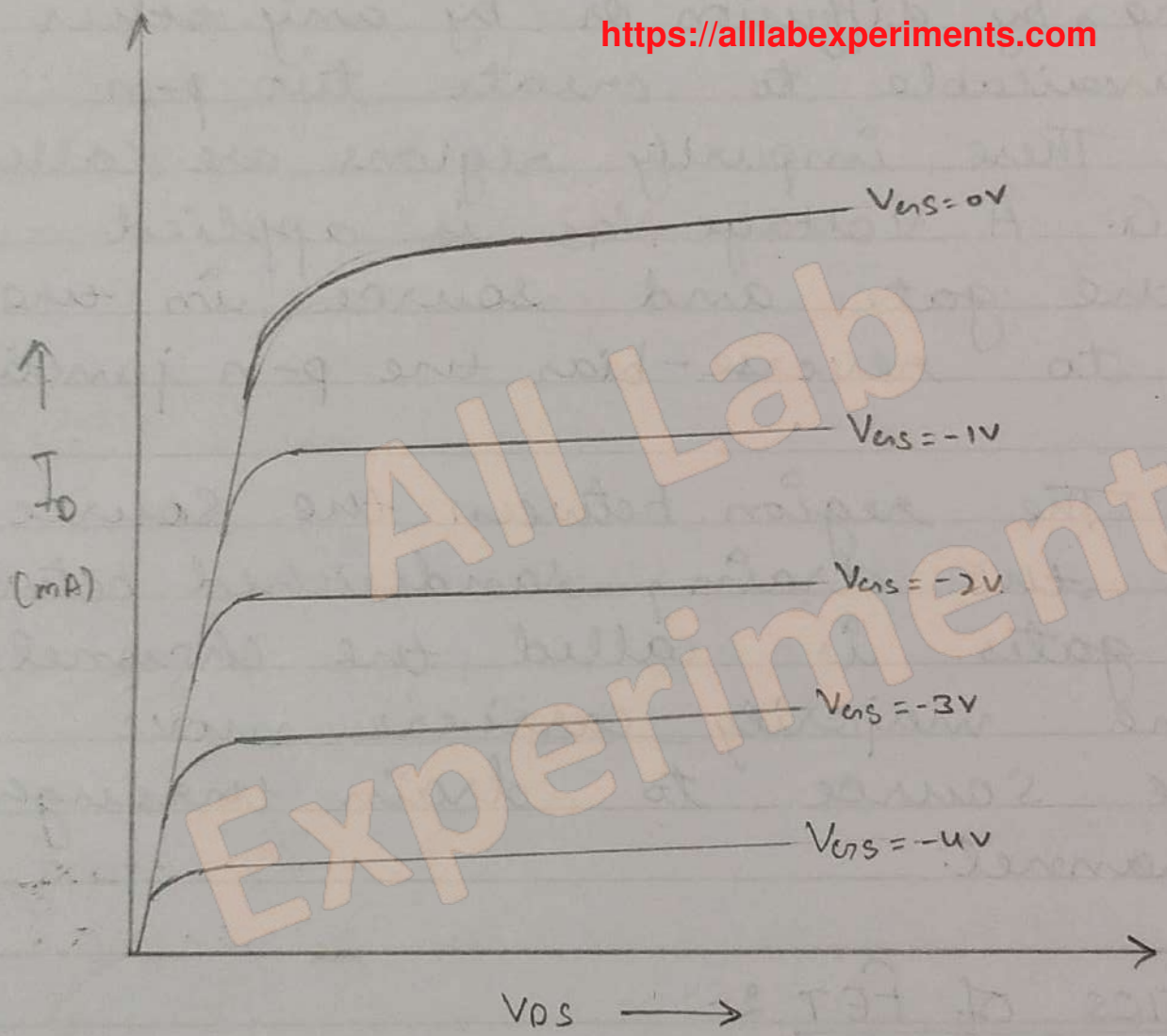
There are two types of static characteristics

① Output or Drain

② Transfer

In the common Source configuration, the bias voltages are applied b/w the gate and source and drain and Source. Now, we discuss the characteristic curve for common Source configuration.

Teacher's Signature : _____



FAMILY OF V-I CHARACTERISTICS OF JFET

Output or Drain Characteristics :-

The curve drawen between drain current I_D and drain - source voltage V_{DS} with gate to source voltage V_{GS} as the parameter is called the Drain curve.

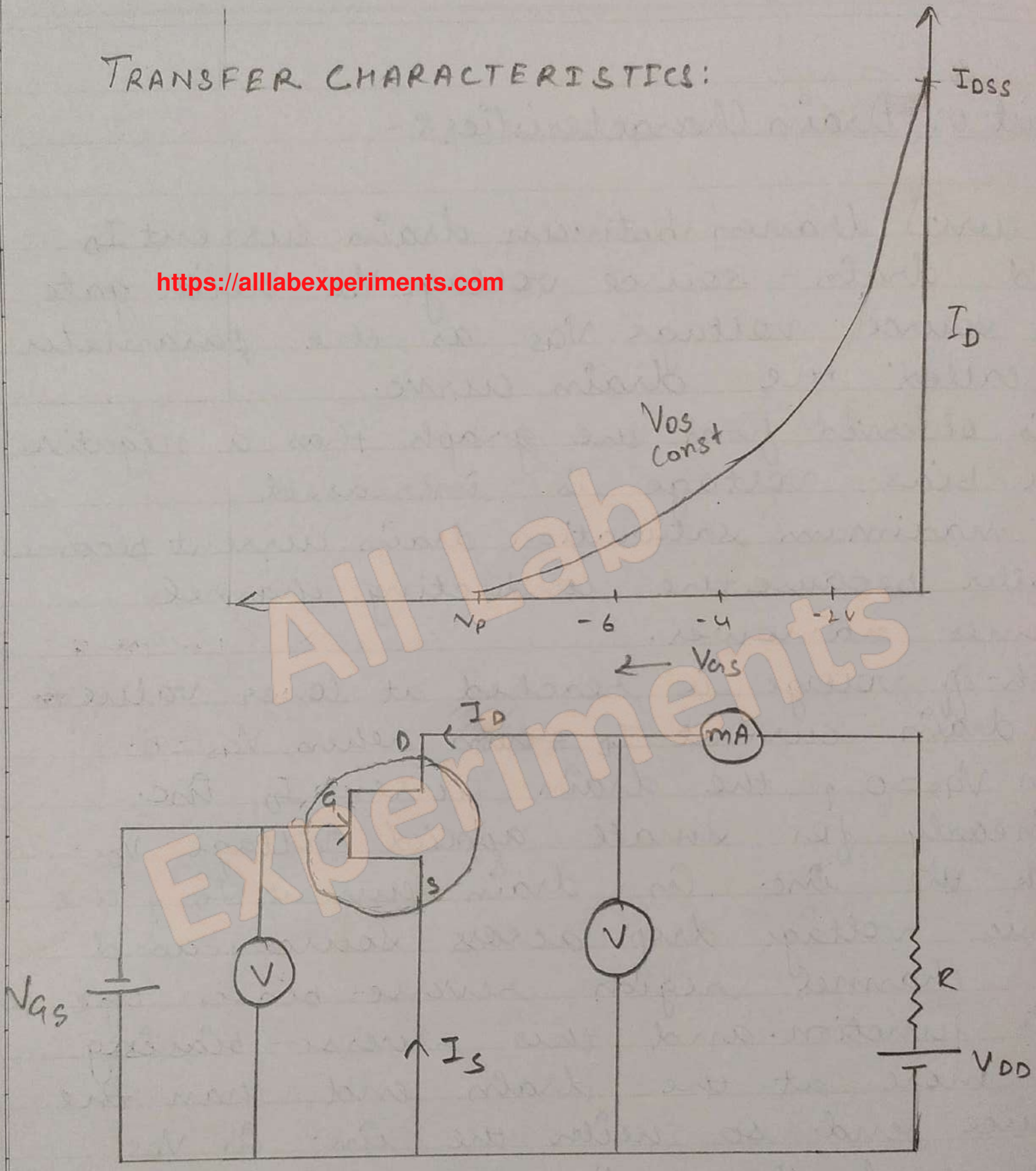
It is observed from the graph that a negative gate bias voltage is increased

(i) the maximum saturation drain current becomes smaller because the conducting channel becomes narrower.

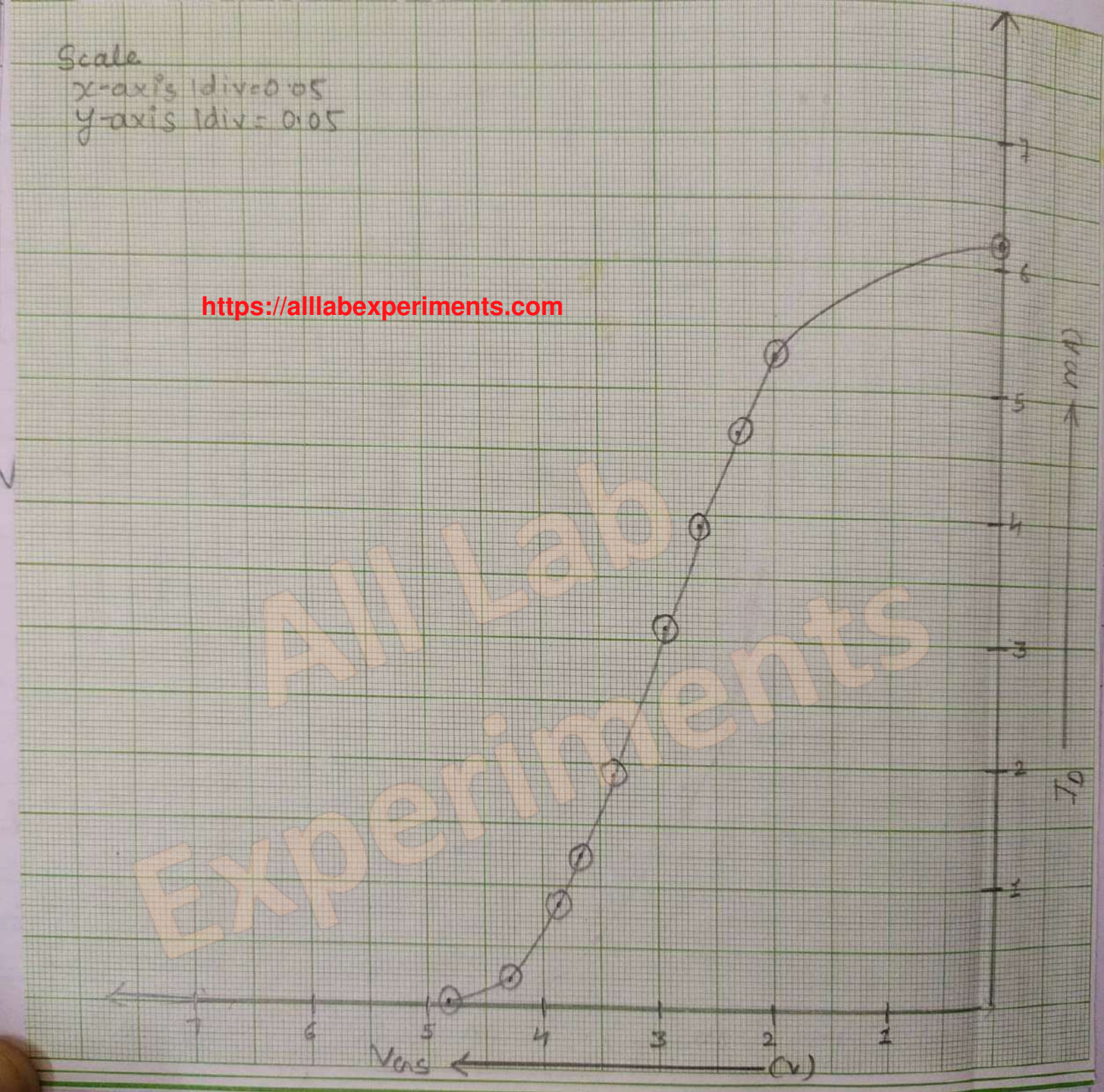
(ii) Pinch-off voltage is reached at lower value of drain current I_D than when $V_{GS}=0$.

When $V_{GS}=0$, the drain current I_D inc. linearly for small applied voltage V_{DS} with the inc. in drain current I_D, the ohmic voltage drop across source and the channel region reverse-biases the gate junction. and this reverse-biasing is more at the drain end than the source end. so with the inc. in V_{DS} the conducting portion of the channel begins to constric more than at the drain end. Eventually a voltage V_{DS} is reached at which the channel is pinched off. The I_D current no longer inc. with the inc. in V_{DS}. It reaches a constant saturation value.

TRANSFER CHARACTERISTICS:



Scale
x-axis 1div=0·05
y-axis 1div = 0·05



TRANSFER CHARACTERISTICS :- The transfer characteristics for JFET can be determined experimentally by keeping drain source voltage V_{DS} constant and determining drain current I_D for various values of gate-source voltage V_{GS}. The curve so plotted is shown in fig on opp. page. It is observed that :-

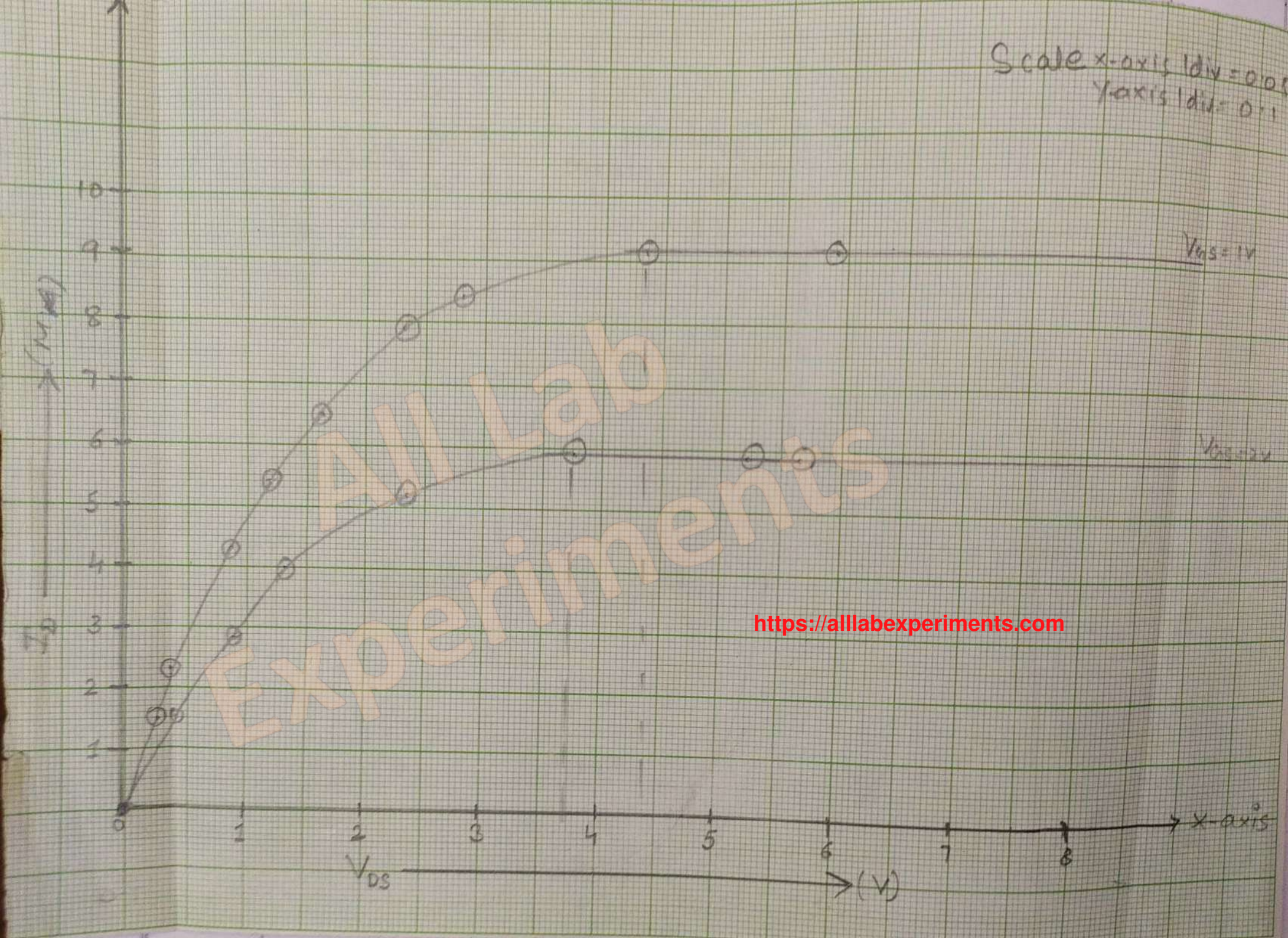
(i) Drain current decreases with the increase in -ve gate-source voltage.
(ii) drain current $I_D = I_{DSS}$ when $V_{GS} = 0$
(iii) drain current $I_D = 0$ when $V_{GS} = V_P$.

PROCEDURE :-

1. Connect the circuit as shown.
2. Fix the gate to source voltage V_{GS} to some suitable value.
3. Vary V_{DS} and note down V_D and I_D
4. Now change the value of V_{GS} and repeat step (3).
5. Now plote I_D versus V_D and trace the curve. The curve obtained is the output/drain characteristic of Common Source FET.
6. Now fix V_{DS} constant to some suitable value.
7. Vary V_{GS} and note down voltage V_G and

S.No	V_{DS} = 1.0 V		V_{DS} = 2 V	
	V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)
1	0	6.23	0	9.87
2	0.03	6.20	0.04	9.85
3	0.13	6.19	0.08	9.84
4	0.29	6.15	0.24	9.76
5	0.54	6.10	0.47	9.59
6	0.71	6.05	0.75	9.32
7	0.92	6.00	0.94	9.02
8	2.01	5 31	1.77	6.58
9	2.66	3.83	2.36	4.67
10	3.25	2.28	2 86	3.29
11	4.27	0.31	4.25	0.38
12	4.36	0.21	4.39	0.20
13	4.49	0.09	4.54	0.08
14	4.68	0.01	4.68	0.01
15	4.72	0	4.73	0

S.NO	V_{GS} = 1V		V_{GS} = 2V	
	V_{DS} (V)	I_D(mA)	V_{DS}(V)	I_D(mA)
1	.01	0.10	0.02	0.11
2	0.06	0.34	0.13	0.52
3	0.17	0.93	0.34	1.31
4	0.39	1.54	1.08	1 38
5	1.22	2.44	2.38	3.49
6	2.30	4.18	3.28	5.25
7	4.39	8.42	3.73	5.47
8	5.60	9.19	5.32	5 82
9	5 79	9.20	5.40	5.84
10	5.90	9.22	5 51	5.85
11				



current I_D.

(8) Now change the value of V_{DS} and repeat step (7).

(9) Now plot I_D versus V_G and trace the curve. The curve obtained is the transfer / input characteristic curve for common Source FET.

RESULT :- The I-V characteristic of common Source FET has been studied and evaluated.